Please type a plus sign (+) inside this box → [+]

PTO/SB/05 (12/97)

UTILITY PATENT APPLICATION TRANSMITTAL

(only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Attorney Docket No.	402/568
First Named Inventor or Application Identifier	Yutaka Murakami et al.
Title	MODULATION METHOD AND RADIO COMMUNICATION SYSTEM
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: **Assistant Commissioner for Patents**
Box Applications
Washington, DC 20231

1. [X] Filing Fee as calculated below.
2. [X] Specification [Total Pages [114]]
   (preferred arrangement set forth below)
   - Descriptive title of the invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [Total Pages [46]]
4. Oath or Declaration [Total Pages [2]]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)*
      [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other:

17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No. ____/____

18. CORRESPONDENCE ADDRESS

[ ] Customer Number or Bar Code Label *(Insert Customer No. or Attach bar code label here)* or [X] Correspondence address below

NAME	**Pollock, Vande Sande & Amernick, R.L.L.P.**				
ADDRESS	**Suite 800**				
	1990 M Street, N.W.				
CITY	**Washington**	STATE	**DC**	ZIP CODE	**20036-3425**
COUNTRY	**U.S.A**	TELEPHONE	**(202) 331-7111**	FAX	**(202) 293-6229**

Fee Calculation and Transmittal

	(Col 1) NO. FILED		(Col 2)	(Col 3) NO. EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE	OR	NON-SMALL ENTITY RATE	NON-SMALL ENTITY FEE
TOTAL	35	minus	20	= 15	x9=	$		x18=	$270
INDEP	4	minus	3	= 1	x39=	$		x78=	$78
___ First Presentation, Multiple Dependent Claims					+130=	$		+260=	$0
Base Filing Fee						$380			$760
Other Fee (specify purpose) Assignment recordation						$			$40
TOTAL FILING FEE* (accounting for possible small entity status)						$	OR	TOTAL	$1,148

☒ A check in the amount of $1,148.00 to cover the filing fee is enclosed

☐ No payment is enclosed at this time. Full payment will be made when the executed Declaration is submitted.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. 22-0185 as described below. A duplicate copy of this sheet is enclosed.

- ☐ Charge the amount of _____ as filing fee
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 CFR § 1.16 and 1.17
- ☐ Charge the Issue Fee set in 37 CFR § 1.18 at the mailing of the Notice of Allowance, pursuant to 37 CFR § 1.311(b)

Name *(Print/Type)*	Morris Liss	Registration No. *(Attorney/Agent)*	24,510
Signature	Morris Liss	Date	2/1/99

TITLE OF THE INVENTION

MODULATION METHOD AND RADIO COMMUNICATION SYSTEM

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a modulation method. This invention also relates to a radio communication system.

Description of the Related Art

Japanese published unexamined patent application 9-93302 discloses a digital radio communication system in which a transmitted signal is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first and second symbols are pilot symbols of known data (fixed data), and the pilot symbols are followed by (N-2) symbols representing main information to be transmitted.

In the digital radio communication system of Japanese application 9-93302, since pilot symbols in every frame are composed of fixed data and are not used in the transmission of main information, they cause a decrease in the main-information transmission rate.

SUMMARY OF THE INVENTION

It is a first object of this invention to provide a modulation method which can prevent the occurrence of a decrease in an information transmission rate.

It is a second object of this invention to provide a radio communication system which can prevent the occurrence of a

decrease in an information transmission rate.

A first aspect of this invention provides a method of modulation which comprises the steps of periodically and alternately subjecting an input digital signal to first modulation and second modulation to convert the input digital signal into a pair of a baseband I signal and a baseband Q signal, the first modulation and the second modulation being different from each other; and outputting the pair of the baseband I signal and the baseband Q signal.

A second aspect of this invention is based on the first aspect thereof, and provides a method wherein the first modulation is at least 8-signal-point modulation, and the second modulation is phase shift keying.

A third aspect of this invention is based on the second aspect thereof, and provides a method wherein the phase shift keying is quadrature phase shift keying.

A fourth aspect of this invention is based on the third aspect thereof, and provides a method wherein the quadrature phase shift keying provides signal points on an I axis and a Q axis in an I-Q plane.

A fifth aspect of this invention is based on the second aspect thereof, and provides a method wherein the at least 8-signal-point modulation is at least 8 quadrature amplitude modulation.

A sixth aspect of this invention is based on the fourth aspect thereof, and provides a method wherein the at least 8-signal-point modulation is at least 8 quadrature amplitude modulation.

A seventh aspect of this invention is based on the fifth aspect thereof, and provides a method wherein the at least 8 quadrature amplitude modulation is 16 quadrature amplitude modulation.

An eighth aspect of this invention is based on the sixth aspect thereof, and provides a method wherein the at least 8 quadrature amplitude modulation is 16 quadrature amplitude modulation.

A ninth aspect of this invention is based on the fifth aspect thereof, and provides a method wherein the at least 8 quadrature amplitude modulation provides signal points which result from rotation of signal points of at least 8-value normal quadrature amplitude modulation through an angle of $\pi/4$ radian about an origin in an I-Q plane.

A tenth aspect of this invention is based on the sixth aspect thereof, and provides a method wherein the at least 8 quadrature amplitude modulation provides signal points which result from rotation of signal points of at least 8-value normal quadrature amplitude modulation through an angle of $\pi/4$ radian about an origin in an I-Q plane.

An eleventh aspect of this invention is based on the seventh aspect thereof, and provides a method wherein the 16 quadrature amplitude modulation provides signal points which result from rotation of signal points of 16-value normal quadrature amplitude modulation through an angle of $\pi/4$ radian about an origin in an I-Q plane.

A twelfth aspect of this invention is based on the eighth aspect thereof, and provides a method wherein the 16 quadrature

amplitude modulation provides signal points which result from rotation of signal points of 16-value normal quadrature amplitude modulation through an angle of $\pi/4$ radian about an origin in an I-Q plane.

A thirteenth aspect of this invention is based on the second aspect thereof, and provides a method wherein a maximum of amplitudes corresponding to signal points of the at least 8-signal-point modulation in an I-Q plane is equal to an amplitude of a signal point of the phase shift keying in the I-Q plane.

A fourteenth aspect of this invention is based on the seventh aspect thereof, and provides a method wherein a distance between signal points of the 16 quadrature amplitude modulation in an I-Q plane is equal to a given value times a distance between signal points of the phase shift keying in the I-Q plane, the given value being in a range of 0.9 to 1.5.

A fifteenth aspect of this invention is based on the seventh aspect thereof, and provides a method wherein a distance between signal points of the 16 quadrature amplitude modulation in an I-Q plane is equal to twice a distance between signal points of the phase shift keying in the I-Q plane.

A sixteenth aspect of this invention is based on the eighth aspect thereof, and provides a method wherein a distance between signal points of the 16 quadrature amplitude modulation in the I-Q plane is equal to $\sqrt{2}$ times a distance between signal points of the quadrature phase shift keying in the I-Q plane.

A seventeenth aspect of this invention is based on the second

aspect thereof, and provides a method wherein the phase shift keying providing periodically-spaced symbols which represent corresponding portions of the input digital signal in terms of differences between phases of the periodically-spaced symbols.

An eighteenth aspect of this invention is based on the seventeenth aspect thereof, and provides a method wherein the at least 8-signal-point modulation assigns logic states of the input digital signal to respective signal points for a first symbol in response to a signal point used by a second symbol of the phase shift keying which precedes the first symbol.

A nineteenth aspect of this invention is based on the seventeenth aspect thereof, and provides a method wherein the at least 8-signal-point modulation is at least 8 quadrature amplitude modulation.

A twentieth aspect of this invention is based on the nineteenth aspect thereof, and provides a method wherein the at least 8 quadrature amplitude modulation is 16 quadrature amplitude modulation.

A twenty-first aspect of this invention is based on the nineteenth aspect thereof, and provides a method wherein the at least 8 quadrature amplitude modulation provides signal points which result from rotation of signal points of at least 8-value normal quadrature amplitude modulation through an angle of $\pi/4$ radian about an origin in an I-Q plane.

A twenty-second aspect of this invention is based on the twentieth aspect thereof, and provides a method wherein the 16

EP 0 752 768 A2

quadrature amplitude modulation provides signal points which result from rotation of signal points of 16-value normal quadrature amplitude modulation through an angle of $\pi/4$ radian about an origin in an I-Q plane.

A twenty-third aspect of this invention is based on the seventeenth aspect thereof, and provides a method wherein the phase shift keying is quadrature phase shift keying.

A twenty-fourth aspect of this invention is based on the twenty-third aspect thereof, and provides a method wherein the quadrature phase shift keying provides signal points on an I axis and a Q axis in an I-Q plane.

A twenty-fifth aspect of this invention is based on the first aspect thereof, and provides a method wherein the first modulation is 16 quadrature amplitude modulation, and the second modulation is quadrature phase shift keying.

A twenty-sixth aspect of this invention is based on the twenty-fifth aspect thereof, and provides a method wherein the 16 quadrature amplitude modulation provides signal points which result from rotation of signal points of 16-value normal quadrature amplitude modulation through an angle of $\pi/4$ radian about an origin in an I-Q plane.

A twenty-seventh aspect of this invention is based on the twenty-fifth aspect thereof, and provides a method wherein the quadrature phase shift keying provides signal points on an I axis and a Q axis in an I-Q plane.

A twenty-eighth aspect of this invention is based on the

twenty-fifth aspect thereof, and provides a method wherein the 16 quadrature amplitude modulation provides signal points which result from rotation of signal points of 16-value normal quadrature amplitude modulation through an angle of $\pi/4$ radian about an origin in an I-Q plane, and the quadrature phase shift keying provides signal points on an I axis and a Q axis in the I-Q plane.

A twenty-ninth aspect of this invention is based on the twenty-fifth aspect thereof, and provides a method wherein a maximum of amplitudes corresponding to signal points of the 16 quadrature amplitude modulation in an I-Q plane is equal to an amplitude of a signal point of the quadrature phase shift keying in the I-Q plane.

A thirtieth aspect of this invention is based on the twenty-fifth aspect thereof, and provides a method wherein a distance between signal points of the 16 quadrature amplitude modulation in an I-Q plane is equal to a given value times a distance between signal points of the quadrature phase shift keying in the I-Q plane, the given value being in a range of 0.9 to 1.5.

A thirty-first aspect of this invention is based on the twenty-fifth aspect thereof, and provides a method wherein a distance between signal points of the 16 quadrature amplitude modulation in an I-Q plane is equal to twice a distance between signal points of the quadrature phase shift keying in the I-Q plane.

A thirty-second aspect of this invention is based on the twenty-sixth aspect thereof, and provides a method wherein a distance between signal points of the 16 quadrature amplitude modulation in the I-Q plane is equal to $\sqrt{2}$ times a distance between

signal points of the quadrature phase shift keying in the I-Q plane.

A thirty-third aspect of this invention provides a transmission apparatus comprising first means for periodically and alternately subjecting an input digital signal to first modulation and second modulation to convert the input digital signal into a pair of a baseband I signal and a baseband Q signal, the first modulation and the second modulation being different from each other, the first modulation being at least 8-signal-point modulation, the second modulation being phase shift keying; and second means for outputting the pair of the baseband I signal and the baseband Q signal.

A thirty-fourth aspect of this invention provides a reception apparatus comprising first means for recovering a pair of a baseband I signal and a baseband Q signal from a received signal; and second means for periodically and alternately subjecting the pair of the baseband I signal and the baseband Q signal to first demodulation and second demodulation to convert the pair of the baseband I signal and the baseband Q signal into an original digital signal; wherein the first demodulation is for signals of at least 8 signal points modulation, and the second demodulation is phase shift keying demodulation.

A thirty-fifth aspect of this invention provides a radio communication system comprising a transmission apparatus including a1) first means for periodically and alternately subjecting an input digital signal to first modulation and second modulation to convert the input digital signal into a pair of a baseband I signal and

a baseband Q signal, the first modulation and the second modulation being different from each other, the first modulation being at least 8-signal-point modulation, the second modulation being phase shift keying; a2) second means for converting the pair of the baseband I signal and the baseband Q signal generated by the first means into a corresponding RF signal; and a3) third means for transmitting the RF signal generated by the second means; a reception apparatus including b1) fourth means for receiving the RF signal transmitted by the third means; b2) fifth means for recovering a pair of a baseband I signal and a baseband Q signal from the RF signal received by the fourth means; and b3) sixth means for periodically and alternately subjecting the pair of the baseband I signal and the baseband Q signal recovered by the fifth means to first demodulation and second demodulation to convert the pair of the baseband I signal and the baseband Q signal into an original digital signal; wherein the first demodulation is for signals of at least 8 signal points modulation, and the second demodulation is phase shift keying demodulation.

0950303-050905

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a transmitter in a radio communication system according to a first embodiment of this invention.

Fig. 2 is a block diagram of a modulator (a quadrature baseband modulator) in Fig. 1.

Fig. 3 is a block diagram of a receiver in the radio communication system according to the first embodiment of this

invention.

Fig. 4 is a block diagram of a quasi synchronous detector in Fig. 3.

Fig. 5 is a diagram of an arrangement of 16 signal points in an I-Q plane which are provided by 16-value APSK.

Fig. 6 is a diagram of an arrangement of signal points in an I-Q plane which are provided by QPSK.

Fig. 7 is a time-domain diagram of a symbol stream.

Fig. 8 is a bock diagram of a modulator (a quadrature baseband modulator) in a transmitter in a radio communication system according to a second embodiment of this invention.

Fig. 9 is a bock diagram of a quasi synchronous detector in a receiver in the radio communication system according to the second embodiment of this invention.

Fig. 10 is a diagram of an arrangement of signal points in an I-Q plane which are provided by 2^{2m}QAM (2^{2m}-value QAM).

Fig. 11 is a time-domain diagram of a symbol stream.

Fig. 12 is a diagram of an arrangement of signal points in an I-Q plane which are provided by 16QAM (16-value QAM).

Fig. 13 is a time-domain diagram of a symbol stream.

Fig. 14 is a block diagram of a modulator (a quadrature baseband modulator) in a transmitter in a radio communication system according to a fourth embodiment of this invention.

Fig. 15 is a diagram of an arrangement of signal points in an I-Q plane which are provided by QPSK.

Fig. 16 is a block diagram of a quasi synchronous detector in a

receiver in the radio communication system according to the fourth embodiment of this invention.

Fig. 17 is a block diagram of a modulator (a quadrature baseband modulator) in a transmitter in a radio communication system according to a fifth embodiment of this invention.

Fig. 18 is a block diagram of a quasi synchronous detector in a receiver in the radio communication system according to the fifth embodiment of this invention.

Fig. 19 is a block diagram of a modulator (a quadrature baseband modulator) in a transmitter in a radio communication system according to a seventh embodiment of this invention.

Fig. 20 is a block diagram of a quasi synchronous detector in a receiver in the radio communication system according to the seventh embodiment of this invention.

Fig. 21 is a diagram of an arrangement of signal points in an I-Q plane which are provided by 2^{2m}QAM (2^{2m}-value QAM).

Fig. 22 is a diagram of an arrangement of signal points in an I-Q plane which are provided by 16QAM (16-value QAM).

Fig. 23 is a block diagram of a modulator (a quadrature baseband modulator) in a transmitter in a radio communication system according to a ninth embodiment of this invention.

Fig. 24 is a block diagram of a quasi synchronous detector in a receiver in the radio communication system according to the ninth embodiment of this invention.

Fig. 25 is a time-domain diagram of a symbol stream.

Fig. 26 is a diagram of the relation between the bit error rate

and the carrier-to-noise power ratio which is provided in an eleventh embodiment of this invention, and the corresponding relation in a prior-art system.

Fig. 27 is a diagram of the relation between the bit error rate and the carrier-to-noise power ratio which is provided in a twelfth embodiment of this invention, and the corresponding relation in a prior-art system.

Fig. 28 is a diagram of the relation between the bit error rate and the carrier-to-noise power ratio which is provided in a thirteenth embodiment of this invention, and the corresponding relation in a prior-art system.

Fig. 29 is a diagram of the relation between the bit error rate and the carrier-to-noise power ratio which is provided in a fourteenth embodiment of this invention, and the corresponding relation in a prior-art system.

Fig. 30 is a block diagram of a transmitter in a radio communication system according to a fifteenth embodiment of this invention.

Fig. 31 is a block diagram of a modulator (a quadrature baseband modulator) in Fig. 30.

Fig. 32 is a block diagram of a receiver in the radio communication system according to the fifteenth embodiment of this invention.

Fig. 33 is a block diagram of a quasi synchronous detector in Fig. 32.

Fig. 34 is a diagram of an arrangement of 8 signal points in an

I-Q plane which are provided by 8PSK.

Fig. 35 is a diagram of an arrangement of two signal points in an I-Q plane which are provided by BPSK.

Fig. 36 is a time-domain diagram of a symbol stream.

Fig. 37 is a diagram of an arrangement of signal points of BPSK, and logic states assigned thereto.

Fig. 38 is a diagram of signal points of 8PSK, logic states assigned thereto, and a first signal point of BPSK.

Fig. 39 is a diagram of signal points of 8PSK, logic states assigned thereto, and a second signal point of BPSK.

Fig. 40 is a block diagram of a modulator (a quadrature baseband modulator) in a transmitter in a radio communication system according to a sixteenth embodiment of this invention.

Fig. 41 is a block diagram of a quasi synchronous detector in a receiver in the radio communication system according to the sixteenth embodiment of this invention.

Fig. 42 is a diagram of an arrangement of signal points in an I-Q plane which are provided by 2^{2m}QAM (2^{2m}-value QAM).

Fig. 43 is a diagram of an arrangement of signal points in an I-Q plane which are provided by 16QAM (16-value QAM).

Fig. 44 is a time-domain diagram of a symbol stream.

Fig. 45 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a first signal point of BPSK.

Fig. 46 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a second signal point of BPSK.

Fig. 47 is a block diagram of a modulator (a quadrature

baseband modulator) in a transmitter in a radio communication system according to a seventeenth embodiment of this invention.

Fig. 48 is a block diagram of a quasi synchronous detector in a receiver in the radio communication system according to the seventeenth embodiment of this invention.

Fig. 49 is a diagram of an arrangement of signal points in an I-Q plane which are provided by 2^{2m}QAM (2^{2m}-value QAM).

Fig. 50 is a diagram of an arrangement of signal points in an I-Q plane which are provided by 16QAM (16-value QAM).

Fig. 51 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a first signal point of BPSK.

Fig. 52 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a second signal point of BPSK.

Fig. 53 is a block diagram of a modulator (a quadrature baseband modulator) in a transmitter in a radio communication system according to an eighteenth embodiment of this invention.

Fig. 54 is a block diagram of a quasi synchronous detector in a receiver in the radio communication system according to the eighteenth embodiment of this invention.

Fig. 55 is a diagram of an arrangement of signal points in an I-Q plane which are provided by QPSK.

Fig. 56 is a time-domain diagram of a symbol stream.

Fig. 57 is a diagram of signal points of QPSK, and logic states assigned thereto.

Fig. 58 is a diagram of signal points of 8PSK, logic states assigned thereto, and a first signal point of QPSK.

EP 0 954 905 A2

Fig. 59 is a diagram of signal points of 8PSK, logic states assigned thereto, and a second signal point of QPSK.

Fig. 60 is a diagram of signal points of 8PSK, logic states assigned thereto, and a third signal point of QPSK.

Fig. 61 is a diagram of signal points of 8PSK, logic states assigned thereto, and a fourth signal point of QPSK.

Fig. 62 is a block diagram of a modulator (a quadrature baseband modulator) in a transmitter in a radio communication system according to a nineteenth embodiment of this invention.

Fig. 63 is a block diagram of a quasi synchronous detector in a receiver in the radio communication system according to the nineteenth embodiment of this invention.

Fig. 64 is a time-domain diagram of a symbol stream.

Fig. 65 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a first signal point of QPSK.

Fig. 66 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a second signal point of QPSK.

Fig. 67 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a third signal point of QPSK.

Fig. 68 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a fourth signal point of QPSK.

Fig. 69 is a block diagram of a modulator (a quadrature baseband modulator) in a transmitter in a radio communication system according to a twentieth embodiment of this invention.

Fig. 70 is a block diagram of a quasi synchronous detector in a receiver in the radio communication system according to the

twentieth embodiment of this invention.

Fig. 71 is a diagram of an arrangement of signal points in an I-Q plane which are provided by QPSK.

Fig. 72 is a diagram of signal points of 8PSK, logic states assigned thereto, and a first signal point of QPSK.

Fig. 73 is a diagram of signal points of 8PSK, logic states assigned thereto, and a second signal point of QPSK.

Fig. 74 is a diagram of signal points of 8PSK, logic states assigned thereto, and a third signal point of QPSK.

Fig. 75 is a diagram of signal points of 8PSK, logic states assigned thereto, and a fourth signal point of QPSK.

Fig. 76 is a block diagram of a modulator (a quadrature baseband modulator) in a transmitter in a radio communication system according to a twenty-first embodiment of this invention.

Fig. 77 is a block diagram of a quasi synchronous detector in a receiver in the radio communication system according to the twenty-first embodiment of this invention.

Fig. 78 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a first signal point of QPSK.

Fig. 79 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a second signal point of QPSK.

Fig. 80 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a third signal point of QPSK.

Fig. 81 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a fourth signal point of QPSK.

Fig. 82 is a block diagram of a modulator (a quadrature

EP 0 926 859 A2

baseband modulator) in a transmitter in a radio communication system according to a twenty-second embodiment of this invention.

Fig. 83 is a block diagram of a quasi synchronous detector in a receiver in the radio communication system according to the twenty-second embodiment of this invention.

Fig. 84 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a first signal point of QPSK.

Fig. 85 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a second signal point of QPSK.

Fig. 86 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a third signal point of QPSK.

Fig. 87 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a fourth signal point of QPSK.

Fig. 88 is a block diagram of a modulator (a quadrature baseband modulator) in a transmitter in a radio communication system according to a twenty-third embodiment of this invention.

Fig. 89 is a block diagram of a quasi synchronous detector in a receiver in the radio communication system according to the twenty-third embodiment of this invention.

Fig. 90 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a first signal point of QPSK.

Fig. 91 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a second signal point of QPSK.

Fig. 92 is a diagram of signal points of 16QAM (16-value QAM), logic states assigned thereto, and a third signal point of QPSK.

Fig. 93 is a diagram of signal points of 16QAM (16-value QAM),

logic states assigned thereto, and a fourth signal point of QPSK.

Fig. 94 is a diagram of relations between the bit error rate and the ratio of the 1-bit signal energy "Eb" to the noise power density "N0".

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following description, 2^{2m}-value QAM means 2^{2m}QAM, and 16-value QAM means 16QAM and 16-value APSK means 16APSK.

First Embodiment

Fig. 1 shows a transmitter 10 in a radio communication system according to a first embodiment of this invention. With reference to Fig. 1, the transmitter 10 includes a modulator 12 and an RF (radio frequency) portion 15. The modulator 12 is defined and referred to as the quadrature baseband modulator 12.

A digital signal to be transmitted (that is, an input digital signal or main information to be transmitted) is fed to the quadrature baseband modulator 12. The device 12 subjects the input digital signal to quadrature baseband modulation, thereby converting the input digital signal into a pair of modulation-resultant baseband signals, that is, a baseband I (in-phase) signal and a baseband Q (quadrature) signal. The quadrature baseband modulator 12 outputs the baseband I signal and the baseband Q signal to the RF portion 15.

The RF portion 15 converts the baseband I signal and the baseband Q signal into an RF signal through frequency conversion which may include RF modulation. The RF portion 15 feeds the RF

signal to an antenna 17. The RF signal is radiated by the antenna 17.

As shown in Fig. 2, the quadrature baseband modulator 12 includes a 16-value APSK (amplitude phase shift keying) modulator 12A, a QPSK (quadrature phase shift keying) modulator 12B, a reference signal generator 12C, and switches 12D and 12E.

The APSK modulator 12A and the QPSK modulator 12B receives the input digital signal. The device 12A subjects the input digital signal to 16APSK (16-value APSK modulation), thereby converting the input digital signal into a pair of a baseband I signal and a baseband Q signal. The APSK modulator 12A outputs the baseband I signal to the switch 12D. The APSK modulator 12A outputs the baseband Q signal to the switch 12E. The device 12B subjects the input digital signal to QPSK (QPSK modulation), thereby converting the input digital signal into a pair of a baseband I signal and a baseband Q signal. The QPSK modulator 12B outputs the baseband I signal to the switch 12D. The QPSK modulator 12B outputs the baseband Q signal to the switch 12E. The reference signal generator 12C outputs a reference baseband I signal to the switch 12D. The reference signal generator 12C outputs a reference baseband Q signal to the switch 12E. The output I and Q signals from the reference signal generator 12C are used in acquiring synchronization between the transmitter 10 and a receiver during an initial stage of signal transmission. The switch 12D selects one of the output I signal from the APSK modulator 12A, the output I signal from the QPSK modulator 12B, and the

0950403-0020703

output I signal from the reference signal generator 12C, and transmits the selected I signal to the RF portion 15. The switch 12E selects one of the output Q signal from the APSK modulator 12A, the output Q signal from the QPSK modulator 12B, and the output Q signal from the reference signal generator 12C, and transmits the selected Q signal to the RF portion 15.

During an initial stage of signal transmission, the switch 12D selects the output I signal from the reference signal generator 12C while the switch 12D selects the output Q signal from the reference signal generator 12C. During an interval of time which follows the initial stage, the switch 12D alternately selects one of the output I signal from the APSK modulator 12A and the output I signal from the QPSK modulator 12B at a predetermined period, and transmits the selected I signal to the RF portion 15. During the time interval following the initial stage, the switch 12E alternately selects one of the output Q signal from the APSK modulator 12A and the output Q signal from the QPSK modulator 12B at the predetermined period, and transmits the selected Q signal to the RF portion 15.

Accordingly, with respect to the input digital signal, the quadrature baseband modulator 12 alternately implements the 16-value APSK modulation and the QPSK modulation at the predetermined period.

Fig. 3 shows a receiver 20 in the radio communication system according to the first embodiment of this invention. With reference to Fig. 3, the receiver 20 includes an RF portion 22, calculators 25 and 26, and a quasi synchronous detector 29.

An RF signal caught by an antenna 21 is applied to the RF portion 22. The RF portion 22 subjects the applied RF signal to frequency conversion (which may include RF demodulation), thereby converting the applied RF signal into a pair of a baseband I signal and a baseband Q signal. The RF portion 22 outputs the baseband I signal and the baseband Q signal to the calculators 25 and 26, and the quasi synchronous detector 29.

The calculator 25 estimates an amplitude distortion amount from the baseband I signal and the baseband Q signal. The calculator 25 informs the quasi synchronous detector 29 of the estimated amplitude distortion amount. The calculator 26 estimates a frequency offset amount from the baseband I signal and the baseband Q signal. The calculator 26 informs the quasi synchronous detector 29 of the estimated frequency offset amount.

The device 29 subjects the baseband I signal and the baseband Q signal to quasi synchronous detection responsive to the estimated amplitude distortion amount and the estimated frequency offset amount, thereby demodulating the baseband I signal and the baseband Q signal into an original digital signal. Thus, the quasi synchronous detector 29 recovers the original digital signal from the baseband I signal and the baseband Q signal. The quasi synchronous detector 29 outputs the recovered original digital signal.

As shown in Fig. 4, the quasi synchronous detector 29 includes a 16-value APSK demodulator 29A, a QPSK demodulator 29B, and a switch 29C.

0524052 - 020495

The APSK demodulator 29A and the QPSK demodulator 29B receive the baseband I and Q signals from the RF portion 22. In addition, the APSK demodulator 29A and the QPSK demodulator 29B are informed of the estimated amplitude distortion amount and the estimated frequency offset amount by the calculators 25 and 26.

The device 29A subjects the baseband I signal and the baseband Q signal to 16-value APSK demodulation responsive to the estimated amplitude distortion amount and the estimated frequency offset amount, thereby demodulating the baseband I signal and the baseband Q signal into an original digital signal. Thus, the APSK demodulator 29A recovers the original digital signal from the baseband I signal and the baseband Q signal. The APSK demodulator 29A outputs the recovered original digital signal to the switch 29C.

The device 29B subjects the baseband I signal and the baseband Q signal to QPSK demodulation responsive to the estimated amplitude distortion amount and the estimated frequency offset amount, thereby demodulating the baseband I signal and the baseband Q signal into an original digital signal. Thus, the QPSK demodulator 29B recovers the original digital signal from the baseband I signal and the baseband Q signal. The QPSK demodulator 29B outputs the recovered original digital signal to the switch 29C.

The switch 29C alternately selects the output digital signal from the APSK demodulator 29A and the output digital signal from the QPSK demodulator 29B in response to a timing signal (a frame and symbol sync signal), and transmits the selected digital signal to a later stage. When the baseband I and Q signals outputted from the

0054052-020498

RF portion 22 to the quasi synchronous detector 29 correspond to a result of the 16-value APSK modulation, the switch 29C selects the output digital signal from the APSK demodulator 29A. When the I and Q signals outputted from the RF portion 22 to the quasi synchronous detector 29 correspond to a result of the QPSK modulation, the switch 29C selects the output digital signal from the QPSK demodulator 29B.

For example, the APSK demodulator 29A includes an amplitude correction circuit (an amplitude compensation circuit) and a frequency correction circuit (a frequency compensation circuit). The amplitude correction circuit compensates for an amplitude distortion of the baseband I signal and the baseband Q signal in response to the estimated amplitude distortion, thereby generating a first compensation-resultant baseband I signal and a first compensation-resultant baseband Q signal. The frequency correction circuit compensates for a frequency offset of the first compensation-resultant baseband I signal and the first compensation-resultant baseband Q signal in response to the estimated frequency offset amount, thereby generating a second compensation-resultant baseband I signal and a second compensation-resultant baseband Q signal. In the APSK demodulator 29A, the second compensation-resultant baseband I signal and the second compensation-resultant baseband Q signal are subjected to the 16-value APSK demodulation, being converted into the original digital signal.

For example, the QPSK demodulator 29B includes an

amplitude correction circuit and a frequency correction circuit. The amplitude correction circuit compensates for an amplitude distortion of the baseband I signal and the baseband Q signal in response to the estimated amplitude distortion, thereby generating a first compensation-resultant baseband I signal and a first compensation-resultant baseband Q signal. The frequency correction circuit compensates for a frequency offset of the first compensation-resultant baseband I signal and the first compensation-resultant baseband Q signal in response to the estimated frequency offset amount, thereby generating a second compensation-resultant baseband I signal and a second compensation-resultant baseband Q signal. In the QPSK demodulator 29B, the second compensation-resultant baseband I signal and the second compensation-resultant baseband Q signal are subjected to the QPSK demodulation, being converted into the original digital signal.

Fig. 5 shows an arrangement of 16 signal points in an I-Q plane which are provided by the 16-value APSK modulation. In Fig. 5, the 16 signal points are denoted by the reference numeral "101". The 16 signal points are assigned to 16 different logic values respectively. The positions (I_{16APSK}, Q_{16APSK}) of the 16 signal points are given by the following equations.

$$I_{16APSK} = h0\{\cos(\frac{\pi}{8})\cos(\frac{k\pi}{4}) - \sin(\frac{\pi}{8})\sin(\frac{k\pi}{4})\} + h1\cos(\frac{k\pi}{4}) \quad \cdots(1)$$

$$Q_{16APSK} = h0\{\cos(\frac{\pi}{8})\sin(\frac{k\pi}{4}) + \sin(\frac{\pi}{8})\cos(\frac{k\pi}{4})\} + h1\sin(\frac{k\pi}{4}) \quad \cdots(2)$$

where "k" denotes a variable integer; (h0, h1) = (0, g1) or (h0, h1) =

(g0, 0); "g0" and "g1" denote predetermined constants respectively; and the constant g1 is greater than the constant g0. With reference to Fig. 5, the signal points on the Q axis correspond to the maximum amplitude which is given by the constant g1.

Fig. 6 shows an arrangement of signal points in an I-Q plane which are provided by the QPSK modulation. In Fig. 6, the signal points are denoted by the reference numeral "201". The signal points are assigned to different logic values respectively. The positions (I_{QPSK}, Q_{QPSK}) of the signal points are given by the following equations.

$$I_{QPSK} = p\{\cos(\frac{\pi}{4})\cos(\frac{k\pi}{2}) - \sin(\frac{\pi}{4})\sin(\frac{k\pi}{2})\} \quad \cdots(3)$$

$$Q_{QPSK} = p\{\cos(\frac{\pi}{4})\sin(\frac{k\pi}{2}) + \sin(\frac{\pi}{4})\cos(\frac{k\pi}{2})\} \quad \cdots(4)$$

where "k" denotes a variable integer, and "p" denotes a predetermined constant. With reference to Fig. 6, all the signal points correspond to a same amplitude given by the constant "p". In addition, all the distances between the neighboring signal points are equal to a same value given by $\sqrt{2p}$. Furthermore, the signal points are spaced at equal angular intervals. Accordingly, a QPSK modulation-resultant signal is suited for detecting an amplitude distortion and a frequency offset.

With reference to Fig. 7, a pair of the I signal and the Q signal outputted from the quadrature baseband modulator 12 in the transmitter 10, or the RF signal outputted from the RF portion 15 in the transmitter 10 is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural

0950353-020495

number. In every frame, the first symbol results from the QPSK modulation, and the second and later symbols result from the 16-value APSK modulation. The first symbol in every frame (that is, the QPSK symbol in every frame) is used by the receiver 20 as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver 20, the calculator 25 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 25 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 26 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 26 estimates a frequency offset amount from the separated pilot symbols.

Preferably, the maximum amplitude g1 provided by the 16-value APSK modulation is equal to the amplitude "p" provided by the QPSK modulation. In this case, the amplitude distortion amount and the frequency offset amount can be accurately estimated.

The quasi synchronous detector 29 in the receiver 20 is designed to implement the following processes. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to the QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q

signals of the RF portion 22 represent a pilot symbol. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to the 16-value APSK demodulation and outputs the APSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a normal symbol different from a pilot symbol.

Second Embodiment

A second embodiment of this invention is similar to the first embodiment thereof except for design changes indicated hereinafter.

As shown in Fig. 8, a modulator (a quadrature baseband modulator) in a transmitter in the second embodiment of this invention includes a 2^{2m}QAM (2^{2m}-value QAM or 2^{2m}-value quadrature amplitude modulation) modulator 12F instead of the 16-value APSK modulator 12A (see Fig. 2). Here, "m" denotes a predetermined integer equal to or greater than "2".

As shown in Fig. 9, a quasi synchronous detector in a receiver in the second embodiment of this invention includes a 2^{2m}-value QAM demodulator 29D instead of the 16-value APSK demodulator 29A (see Fig. 4).

Fig. 10 shows an arrangement of signal points in an I-Q plane which are provided by 2^{2m}-value QAM executed in the QAM modulator 12F. In Fig. 10, the signal points are denoted by the reference numeral "401". The signal points are assigned to different logic values respectively. The positions (I_{QAM}, Q_{QAM}) of the signal points are given by the following equations.

$$I_{QAM} = q(2^{m-1}a1 + 2^{m-2}a2 + \bullet\bullet\bullet + 2^{0}am) \quad \cdots(5)$$

$$Q_{QAM} = q(2^{m-1}b1 + 2^{m-2}b2 + \bullet\bullet\bullet + 2^{0}bm) \quad \cdots(6)$$

where "m" denotes a predetermined integer equal to or greater than "2"; (a1, b1), (a2, b2), ···, (am, bm) are binary code words of "1" and "-1"; and "q" denotes a predetermined constant. With reference to Fig. 10, specified ones of the signal points correspond to the maximum amplitude which is given as follows.

$$(2^{m-1} + 2^{m-2} + \bullet\bullet\bullet + 2^{0})\sqrt{2}q \quad \cdots(7)$$

With reference to Fig. 11, a pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 1), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first symbol results from the QPSK modulation, and the second and later symbols result from the 2^{2m}-value QAM. The first symbol in every frame (that is, the QPSK symbol in every frame) is used by the receiver as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 3), the calculator 25 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 25 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 26 separates pilot symbols

(first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 26 estimates a frequency offset amount from the separated pilot symbols.

Preferably, the maximum amplitude provided by the 2^{2m}-value QAM, that is, the value given by the expression (7), is equal to the amplitude "p" provided by the QPSK modulation. In this case, the amplitude distortion amount and the frequency offset amount can be accurately estimated.

The quasi synchronous detector 29 in the receiver (see Fig. 3) is designed to implement the following processes. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a pilot symbol. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to 2^{2m}-value QAM demodulation and outputs the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a normal symbol different from a pilot symbol.

Third Embodiment

A third embodiment of this invention is similar to the second embodiment thereof except that 16-value QAM replaces 2^{2m}-value QAM.

According to the third embodiment of this invention, a

modulator (a quadrature baseband modulator) in a transmitter includes a 16-value QAM modulator instead of the 2^{2m}-value QAM modulator 12F (see Fig. 8). In addition, a quasi synchronous detector in a receiver includes a 16-value QAM demodulator instead of the 2^{2m}-value QAM demodulator 29D (see Fig. 9).

Fig. 12 shows an arrangement of signal points in an I-Q plane which are provided by the 16-value QAM. In Fig. 12, the signal points are denoted by the reference numeral "601". The signal points are assigned to different logic values respectively. The positions (I_{16QAM}, Q_{16QAM}) of the signal points are given by the following equations.

$$I_{16QAM} = r(2^1 a1 + 2^0 a2) \quad \cdots(8)$$

$$Q_{16QAM} = r(2^1 b1 + 2^0 b2) \quad \cdots(9)$$

where (a1, b1) and (a2, b2) are binary code words of "1" and "−1", and "r" denotes a predetermined constant. With reference to Fig. 12, specified ones of the signal points correspond to the maximum amplitude which is given as follows.

$$(2^1 + 2^0)\sqrt{2}r \quad \cdots(10)$$

In addition, the distances between the neighboring signal points are equal to a same value given by "2r".

With reference to Fig. 13, a pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 1), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first symbol results from the

QPSK modulation, and the second and later symbols result from the 16-value QAM. The first symbol in every frame (that is, the QPSK symbol in every frame) is used by the receiver as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 3), the calculator 25 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 25 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 26 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 26 estimates a frequency offset amount from the separated pilot symbols.

Preferably, the maximum amplitude provided by the 16-value QAM, that is, the value given by the expression (10), is equal to the amplitude "p" provided by the QPSK modulation. In this case, the amplitude distortion amount and the frequency offset amount can be accurately estimated.

The quasi synchronous detector 29 in the receiver (see Fig. 3) is designed to implement the following processes. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to QPSK demodulation and outputs the QPSK-

EP 0 525 694 A2

demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a pilot symbol. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to 16-value QAM demodulation and the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a normal symbol different from a pilot symbol.

In general, the inter-signal-point distance "$\sqrt{2}p$" in the QPSK modulation is equal to a given value times the inter-signal-point distance "2r" in the 16-value QAM. Preferably, the given value is in the range of 0.90 to 1.50. In this case, a sufficiently low bit error rate is provided.

The inter-signal-point distance "$\sqrt{2}p$" in the QPSK modulation may be equal to twice the inter-signal-point distance "2r" in the 16-value QAM. In this case, it is preferable that the quasi synchronous detector in the receiver detects the I-Q-plane amplitude of the output I and Q signals of the RF portion when the output I and Q signals of the RF portion 22 represent a pilot symbol, and that the detected I-Q-plane amplitude is used as an I-Q-plane amplitude threshold value for the 16-value QAM demodulation.

Fourth Embodiment

A fourth embodiment of this invention is similar to the first embodiment thereof except for design changes indicated hereinafter.

As shown in Fig. 14, a modulator (a quadrature baseband modulator) in a transmitter in the fourth embodiment of this

invention includes a QPSK modulator 12G instead of the QPSK modulator 12B (see Fig. 2).

Fig. 15 shows an arrangement of signal points in an I-Q plane which are provided by QPSK modulation implemented by the QPSK modulator 12G. In Fig. 15, the signal points are denoted by the reference numeral "801". The signal points are assigned to different logic values respectively. The positions (IQPSKR, QQPSKR) of the signal points are given by the following equations.

$$IQPSKR = IQPSK\{\cos(\frac{\pi}{4} + \frac{n\pi}{2})\} - QQPSK\{\sin(\frac{\pi}{4} + \frac{n\pi}{2})\} \quad \cdots(11)$$

$$QQPSKR = IQPSK\{\sin(\frac{\pi}{4} + \frac{n\pi}{2})\} + QQPSK\{\cos(\frac{\pi}{4} + \frac{n\pi}{2})\} \quad \cdots(12)$$

where "n" denotes an integer, and (IQPSK, QQPSK) are given by the equations (3) and (4). With reference to Fig. 15, all the signal points correspond to a same amplitude given by the constant "p". In addition, all the distances between the neighboring signal points are equal to a same value given by $\sqrt{2p}$. Furthermore, the signal points are spaced at equal angular intervals. Accordingly, a QPSK modulation-resultant signal is suited for detecting an amplitude distortion and a frequency offset.

As shown in Fig. 16, a quasi synchronous detector in a receiver in the fourth embodiment of this invention includes a QPSK demodulator 29E instead of the QPSK demodulator 29B (see Fig. 4). The QPSK demodulator 29E implements demodulation inverse with respect to the modulation by the QPSK modulator 12G.

A pair of the I signal and the Q signal outputted from the quadrature baseband modulator 12 in the transmitter 10 (see Fig.

1), or the RF signal outputted from the RF portion 15 in the transmitter 10 is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first symbol results from the QPSK modulation, and the second and later symbols result from the 16-value APSK modulation. The first symbol in every frame (that is, the QPSK symbol in every frame) is used by the receiver 20 (see Fig. 3) as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver 20, the calculator 25 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 25 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 26 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 26 estimates a frequency offset amount from the separated pilot symbols.

Preferably, the maximum amplitude g1 provided by the 16-value APSK modulation is equal to the amplitude "p" provided by the QPSK modulation. In this case, the amplitude distortion amount and the frequency offset amount can be accurately estimated.

The quasi synchronous detector 29 in the receiver 20 is designed to implement the following processes. The quasi

0524525-052459

synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to the QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a pilot symbol. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to the 16-value APSK demodulation and outputs the APSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a normal symbol different from a pilot symbol.

0 6 2 5 3 6 2 - 0 2 0 5 0 6

Fifth Embodiment

A fifth embodiment of this invention is similar to the second embodiment thereof except for design changes indicated hereinafter.

As shown in Fig. 17, a modulator (a quadrature baseband modulator) in a transmitter in the fifth embodiment of this invention includes a QPSK modulator 12G instead of the QPSK modulator 12B (see Fig. 8). The QPSK modulator 12G implements QPSK modulation providing signal points which are arranged in an I-Q plane as shown in Fig. 15.

As shown in Fig. 18, a quasi synchronous detector in a receiver in the fifth embodiment of this invention includes a QPSK demodulator 29E instead of the QPSK demodulator 29B (see Fig. 9). The QPSK demodulator 29E implements demodulation inverse with respect to the modulation by the QPSK modulator 12G.

A pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 1), or

the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first symbol results from the QPSK modulation, and the second and later symbols result from the 2^{2m}-value QAM. The first symbol in every frame (that is, the QPSK symbol in every frame) is used by the receiver as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 3), the calculator 25 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 25 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 26 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 26 estimates a frequency offset amount from the separated pilot symbols.

Preferably, the maximum amplitude provided by the 2^{2m}-value QAM, that is, the value given by the expression (7), is equal to the amplitude "p" provided by the QPSK modulation. In this case, the amplitude distortion amount and the frequency offset amount can be accurately estimated.

The quasi synchronous detector 29 in the receiver (see Fig. 3) is designed to implement the following processes. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a pilot symbol. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to 2^{2m}-value QAM demodulation and outputs the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a normal symbol different from a pilot symbol.

Sixth Embodiment

A sixth embodiment of this invention is similar to the fifth embodiment thereof except that 16-value QAM replaces 2^{2m}-value QAM.

According to the sixth embodiment of this invention, a modulator (a quadrature baseband modulator) in a transmitter includes a 16-value QAM modulator instead of the 2^{2m}-value QAM modulator 12F (see Fig. 17). The QAM modulator implements 16-value QAM providing signal points which are arranged in an I-Q plane as shown in Fig. 12. According to the sixth embodiment of this invention, a quasi synchronous detector in a receiver includes a 16-value QAM demodulator instead of the 2^{2m}-value QAM demodulator 29D (see Fig. 18).

A pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 1), or

the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first symbol results from the QPSK modulation, and the second and later symbols result from the 16-value QAM. The first symbol in every frame (that is, the QPSK symbol in every frame) is used by the receiver as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 3), the calculator 25 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 25 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 26 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 26 estimates a frequency offset amount from the separated pilot symbols.

Preferably, the maximum amplitude provided by the 16-value QAM, that is, the value given by the expression (10), is equal to the amplitude "p" provided by the QPSK modulation. In this case, the amplitude distortion amount and the frequency offset amount can be accurately estimated.

The quasi synchronous detector 29 in the receiver (see Fig. 3) is designed to implement the following processes. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a pilot symbol. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to 16-value QAM demodulation and the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a normal symbol different from a pilot symbol.

In general, the inter-signal-point distance "$\sqrt{2p}$" in the QPSK modulation is equal to a given value times the inter-signal-point distance "2r" in the 16-value QAM. Preferably, the given value is in the range of 0.90 to 1.50. In this case, a sufficiently low bit error rate is provided.

The inter-signal-point distance "$\sqrt{2p}$" in the QPSK modulation may be equal to twice the inter-signal-point distance "2r" in the 16-value QAM. In this case, it is preferable that the quasi synchronous detector in the receiver detects the I-Q-plane amplitude of the output I and Q signals of the RF portion when the output I and Q signals of the RF portion 22 represent a pilot symbol, and that the detected I-Q-plane amplitude is used as an I-Q-plane amplitude threshold value for the 16-value QAM demodulation.

Seventh Embodiment

A seventh embodiment of this invention is similar to the first

embodiment thereof except for design changes indicated hereinafter.

As shown in Fig. 19, a modulator (a quadrature baseband modulator) in a transmitter in the seventh embodiment of this invention includes a 2^{2m}-value QAM modulator 12H instead of the 16-value APSK modulator 12A (see Fig. 2). Here, "m" denotes a predetermined integer equal to or greater than "2".

As shown in Fig. 20, a quasi synchronous detector in a receiver in the seventh embodiment of this invention includes a 2^{2m}-value QAM demodulator 29F instead of the 16-value APSK demodulator 29A (see Fig. 4).

Fig. 21 shows an arrangement of signal points in an I-Q plane which are provided by 2^{2m}-value QAM executed in the QAM modulator 12H. In Fig. 21, the signal points are denoted by the reference numeral "901". The signal points are assigned to different logic values respectively. The positions of the signal points in Fig. 21 result from rotation of the signal points in Fig. 10 through an angle of $\pi/4$ radian about the origin. Specifically, the positions (I_{QAMR}, Q_{QAMR}) of the signal points in Fig. 21 are given by the following equations.

$$I_{QAMR} = I_{QAM}\{\cos(\frac{\pi}{4} + \frac{n\pi}{2})\} - Q_{QAM}\{\sin(\frac{\pi}{4} + \frac{n\pi}{2})\} \quad \cdots(13)$$

$$Q_{QAMR} = I_{QAM}\{\sin(\frac{\pi}{4} + \frac{n\pi}{2})\} + Q_{QAM}\{\cos(\frac{\pi}{4} + \frac{n\pi}{2})\} \quad \cdots(14)$$

where "n" denotes an integer, and (I_{QAM}, Q_{QAM}) are given by the equations (5) and (6). With reference to Fig. 21, the maximum amplitude which corresponds to specified ones of the signal points

is equal to the value given by the expression (7).

A pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 1), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first symbol results from the QPSK modulation, and the second and later symbols result from the 2^{2m}-value QAM. The first symbol in every frame (that is, the QPSK symbol in every frame) is used by the receiver as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 3), the calculator 25 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 25 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 26 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 26 estimates a frequency offset amount from the separated pilot symbols.

Preferably, the maximum amplitude provided by the 2^{2m}-value QAM, that is, the value given by the expression (7), is equal to

the amplitude "p" provided by the QPSK modulation. In this case, the amplitude distortion amount and the frequency offset amount can be accurately estimated.

The quasi synchronous detector 29 in the receiver (see Fig. 3) is designed to implement the following processes. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a pilot symbol. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to 2^{2m}-value QAM demodulation and outputs the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a normal symbol different from a pilot symbol.

0960-0260-0960

Eighth Embodiment

An eighth embodiment of this invention is similar to the seventh embodiment thereof except that 16-value QAM replaces 2^{2m}-value QAM.

According to the eighth embodiment of this invention, a modulator (a quadrature baseband modulator) in a transmitter includes a 16-value QAM modulator instead of the 2^{2m}-value QAM modulator 12H (see Fig. 19). In addition, a quasi synchronous detector in a receiver includes a 16-value QAM demodulator instead of the 2^{2m}-value QAM demodulator 29F (see Fig. 20).

Fig. 22 shows an arrangement of signal points in an I-Q plane which are provided by 16-value QAM executed in the 16-value QAM

modulator. In Fig. 22, the signal points are denoted by the reference numeral "1001". The signal points are assigned to different logic values respectively. The positions of the signal points in Fig. 22 result from rotation of the signal points in Fig. 12 through an angle of $\pi/4$ radian about the origin. Specifically, the positions (I_{16QAMR}, Q_{16QAMR}) of the signal points in Fig. 22 are given by the following equations.

$$I_{16QAMR} = I_{16QAM}\{\cos(\frac{\pi}{4} + \frac{n\pi}{2})\} - Q_{16QAM}\{\sin(\frac{\pi}{4} + \frac{n\pi}{2})\} \quad \cdots(15)$$

$$Q_{16QAMR} = I_{16QAM}\{\sin(\frac{\pi}{4} + \frac{n\pi}{2})\} + Q_{16QAM}\{\cos(\frac{\pi}{4} + \frac{n\pi}{2})\} \quad \cdots(16)$$

where "n" denotes an integer, and (I_{16QAM}, Q_{16QAM}) are given by the equations (8) and (9). With reference to Fig. 22, the maximum amplitude which corresponds to specified ones of the signal points is equal to the value given by the expression (10). In addition, the distances between the neighboring signal points are equal to a same value given by "2r".

A pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 1), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first symbol results from the QPSK modulation, and the second and later symbols result from the 16-value QAM. The first symbol in every frame (that is, the QPSK symbol in every frame) is used by the receiver as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every

pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 3), the calculator 25 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 25 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 26 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 26 estimates a frequency offset amount from the separated pilot symbols.

Preferably, the maximum amplitude provided by the 16-value QAM, that is, the value given by the expression (10), is equal to the amplitude "p" provided by the QPSK modulation. In this case, the amplitude distortion amount and the frequency offset amount can be accurately estimated.

The quasi synchronous detector 29 in the receiver (see Fig. 3) is designed to implement the following processes. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a pilot symbol. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to 16-value QAM demodulation and the QAM-

demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a normal symbol different from a pilot symbol.

In general, the inter-signal-point distance "$\sqrt{2}$p" in the QPSK modulation is equal to a given value times the inter-signal-point distance "2r" in the 16-value QAM. Preferably, the given value is in the range of 0.90 to 1.50. In this case, a sufficiently low bit error rate is provided.

The inter-signal-point distance "$\sqrt{2}$p" in the QPSK modulation may be equal to "$\sqrt{2}$" times the inter-signal-point distance "2r" in the 16-value QAM. In this case, it is preferable that the quasi synchronous detector in the receiver detects the I-Q-plane amplitude of the output I and Q signals of the RF portion when the output I and Q signals of the RF portion 22 represent a pilot symbol, and that the detected I-Q-plane amplitude is used as an I-Q-plane amplitude threshold value for the 16-value QAM demodulation.

EP 0 525 735 A2

Ninth Embodiment

A ninth embodiment of this invention is similar to the seventh embodiment thereof except for design changes indicated hereinafter.

As shown in Fig. 23, a modulator (a quadrature baseband modulator) in a transmitter in the ninth embodiment of this invention includes a QPSK modulator 12G instead of the QPSK modulator 12B (see Fig. 19). The QPSK modulator 12G implements QPSK modulation providing signal points which are arranged in an I-Q plane as shown in Fig. 15.

As shown in Fig. 24, a quasi synchronous detector in a receiver in the ninth embodiment of this invention includes a QPSK demodulator 29E instead of the QPSK demodulator 29B (see Fig. 20). The QPSK demodulator 29E implements demodulation inverse with respect to the modulation by the QPSK modulator 12G.

A pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 1), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first symbol results from the QPSK modulation, and the second and later symbols result from the 2^{2m}-value QAM. The first symbol in every frame (that is, the QPSK symbol in every frame) is used by the receiver as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 3), the calculator 25 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 25 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 26 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 26

estimates a frequency offset amount from the separated pilot symbols.

Preferably, the maximum amplitude provided by the 2^{2m}-value QAM, that is, the value given by the expression (7), is equal to the amplitude "p" provided by the QPSK modulation. In this case, the amplitude distortion amount and the frequency offset amount can be accurately estimated.

The quasi synchronous detector 29 in the receiver (see Fig. 3) is designed to implement the following processes. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a pilot symbol. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to 2^{2m}-value QAM demodulation and outputs the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a normal symbol different from a pilot symbol.

Tenth Embodiment

A tenth embodiment of this invention is similar to the ninth embodiment thereof except that 16-value QAM replaces 2^{2m}-value QAM.

According to the tenth embodiment of this invention, a modulator (a quadrature baseband modulator) in a transmitter includes a 16-value QAM modulator instead of the 2^{2m}-value QAM modulator 12H (see Fig. 23). The 16-value QAM modulator

implements 16-value QAM providing signal points which are arranged in an I-Q plane as shown in Fig. 22. According to the tenth embodiment of this invention, a quasi synchronous detector in a receiver includes a 16-value QAM demodulator instead of the 2^{2m}-value QAM demodulator 29F (see Fig. 24). The 16-value QAM demodulator implements demodulation inverse with respect to the modulation by the 16-value QAM modulator.

A pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 1), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first symbol results from the QPSK modulation, and the second and later symbols result from the 16-value QAM. The first symbol in every frame (that is, the QPSK symbol in every frame) is used by the receiver as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 3), the calculator 25 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 25 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 26 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF

portion 22 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 26 estimates a frequency offset amount from the separated pilot symbols.

Preferably, the maximum amplitude provided by the 16-value QAM, that is, the value given by the expression (10), is equal to the amplitude "p" provided by the QPSK modulation. In this case, the amplitude distortion amount and the frequency offset amount can be accurately estimated.

The quasi synchronous detector 29 in the receiver (see Fig. 3) is designed to implement the following processes. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a pilot symbol. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to 16-value QAM demodulation and the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a normal symbol different from a pilot symbol.

In general, the inter-signal-point distance "$\sqrt{2p}$" in the QPSK modulation is equal to a given value times the inter-signal-point distance "2r" in the 16-value QAM. Preferably, the given value is in the range of 0.90 to 1.50. In this case, a sufficiently low bit error rate is provided.

The inter-signal-point distance "$\sqrt{2p}$" in the QPSK modulation

may be equal to twice the inter-signal-point distance "2r" in the 16-value QAM. In this case, it is preferable that the quasi synchronous detector in the receiver detects the I-Q-plane amplitude of the output I and Q signals of the RF portion when the output I and Q signals of the RF portion 22 represent a pilot symbol, and that the detected I-Q-plane amplitude is used as an I-Q-plane amplitude threshold value for the 16-value QAM demodulation.

Eleventh Embodiment

An eleventh embodiment of this invention is similar to the third embodiment thereof except for design changes indicated hereinafter.

With reference to Fig. 25, a pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 1), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, first alternate symbols result from the QPSK modulation, and second alternate symbols result from the 16-value QAM. The QPSK symbols in every frame are used by the receiver as pilot symbols for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 3), the calculator 25 separates pilot symbols from the output I and Q signals of the RF portion 22 in response to a signal (a 2-symbol sync signal) having a period

corresponding to two symbols. The calculator 25 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 26 separates pilot symbols from the output I and Q signals of the RF portion 22 in response to a signal (a 2-symbol sync signal) having a period corresponding to 2 symbols. The calculator 26 estimates a frequency offset amount from the separated pilot symbols.

Preferably, the maximum amplitude provided by the 16-value QAM, that is, the value given by the expression (10), is equal to the amplitude "p" provided by the QPSK modulation. In this case, the amplitude distortion amount and the frequency offset amount can be accurately estimated.

The quasi synchronous detector 29 in the receiver (see Fig. 3) is designed to implement the following processes. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a pilot symbol. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to 16-value QAM demodulation and the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a normal symbol different from a pilot symbol.

In general, the inter-signal-point distance "$\sqrt{2p}$" in the QPSK modulation is equal to a given value times the inter-signal-point distance "2r" in the 16-value QAM. Preferably, the given value is in

the range of 0.90 to 1.50. In this case, a sufficiently low bit error rate is provided.

With reference to Fig. 26, in the case where the inter-signal-point distance "$\sqrt{2}p$" in the QPSK modulation is equal to 1.20 times the inter-signal-point distance "2r" in the 16-value QAM, the bit error rate provided in the embodiment of this invention decreases along the curve A0 as the carrier-to-noise power ratio C/N increases. Fig. 26 also indicates a comparative example being the relation B0 between the bit error rate and the carrier-to-noise power ratio C/N which occurs in a prior-art 8PSK (8 or octonary phase shift keying) system. As shown in Fig. 26, the bit error rate (the curve A0) provided in the embodiment of this invention is better than that in the prior-art 8PSK system.

The inter-signal-point distance "$\sqrt{2}p$" in the QPSK modulation may be equal to twice the inter-signal-point distance "2r" in the 16-value QAM. In this case, it is preferable that the quasi synchronous detector in the receiver detects the I-Q-plane amplitude of the output I and Q signals of the RF portion when the output I and Q signals of the RF portion 22 represent a pilot symbol, and that the detected I-Q-plane amplitude is used as an I-Q-plane amplitude threshold value for the 16-value QAM demodulation.

Twelfth Embodiment

A twelfth embodiment of this invention is similar to the sixth embodiment thereof except for design changes indicated hereinafter.

A pair of the I signal and the Q signal outputted from the

quadrature baseband modulator in the transmitter (see Fig. 1), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, first alternate symbols result from the QPSK modulation, and second alternate symbols result from the 16-value QAM. The QPSK symbols in every frame are used by the receiver as pilot symbols for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 3), the calculator 25 separates pilot symbols from the output I and Q signals of the RF portion 22 in response to a signal (a 2-symbol sync signal) having a period corresponding to two symbols. The calculator 25 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 26 separates pilot symbols from the output I and Q signals of the RF portion 22 in response to a signal (a 2-symbol sync signal) having a period corresponding to 2 symbols. The calculator 26 estimates a frequency offset amount from the separated pilot symbols.

Preferably, the maximum amplitude provided by the 16-value QAM, that is, the value given by the expression (10), is equal to the amplitude "p" provided by the QPSK modulation. In this case, the amplitude distortion amount and the frequency offset amount can be accurately estimated.

The quasi synchronous detector 29 in the receiver (see Fig. 3)

is designed to implement the following processes. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a pilot symbol. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to 16-value QAM demodulation and the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a normal symbol different from a pilot symbol.

In general, the inter-signal-point distance "$\sqrt{2}p$" in the QPSK modulation is equal to a given value times the inter-signal-point distance "2r" in the 16-value QAM. Preferably, the given value is in the range of 0.90 to 1.50. In this case, a sufficiently low bit error rate is provided.

With reference to Fig. 27, in the case where the inter-signal-point distance "$\sqrt{2}p$" in the QPSK modulation is equal to 1.20 times the inter-signal-point distance "2r" in the 16-value QAM, the bit error rate provided in the embodiment of this invention decreases along the curve A1 as the carrier-to-noise power ratio C/N increases. Fig. 27 also indicates a comparative example being the relation B1 between the bit error rate and the carrier-to-noise power ratio C/N which occurs in a prior-art 8PSK (8 or octonary phase shift keying) system. As shown in Fig. 27, the bit error rate (the curve A1) provided in the embodiment of this invention is better than that in the prior-art 8PSK system.

The inter-signal-point distance "$\sqrt{2}p$" in the QPSK modulation may be equal to "$\sqrt{2}$" times the inter-signal-point distance "2r" in the 16-value QAM. In this case, it is preferable that the quasi synchronous detector in the receiver detects the I-Q-plane amplitude of the output I and Q signals of the RF portion when the output I and Q signals of the RF portion 22 represent a pilot symbol, and that the detected I-Q-plane amplitude is used as an I-Q-plane amplitude threshold value for the 16-value QAM demodulation.

Thirteenth Embodiment

A thirteenth embodiment of this invention is similar to the eighth embodiment thereof except for design changes indicated hereinafter.

A pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 1), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, first alternate symbols result from the QPSK modulation, and second alternate symbols result from the 16-value QAM. The QPSK symbols in every frame are used by the receiver as pilot symbols for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 3), the calculator 25 separates pilot symbols from the output I and Q signals of the RF portion 22 in response to a signal (a 2-symbol sync signal) having a period

corresponding to two symbols. The calculator 25 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 26 separates pilot symbols from the output I and Q signals of the RF portion 22 in response to a signal (a 2-symbol sync signal) having a period corresponding to 2 symbols. The calculator 26 estimates a frequency offset amount from the separated pilot symbols.

Preferably, the maximum amplitude provided by the 16-value QAM, that is, the value given by the expression (10), is equal to the amplitude "p" provided by the QPSK modulation. In this case, the amplitude distortion amount and the frequency offset amount can be accurately estimated.

The quasi synchronous detector 29 in the receiver (see Fig. 3) is designed to implement the following processes. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a pilot symbol. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to 16-value QAM demodulation and the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a normal symbol different from a pilot symbol.

In general, the inter-signal-point distance "$\sqrt{2}p$" in the QPSK modulation is equal to a given value times the inter-signal-point distance "2r" in the 16-value QAM. Preferably, the given value is in

the range of 0.90 to 1.50. In this case, a sufficiently low bit error rate is provided.

With reference to Fig. 28, in the case where the inter-signal-point distance "$\sqrt{2p}$" in the QPSK modulation is equal to 1.20 times the inter-signal-point distance "2r" in the 16-value QAM, the bit error rate provided in the embodiment of this invention decreases along the curve A2 as the carrier-to-noise power ratio C/N increases. Fig. 28 also indicates a comparative example being the relation B2 between the bit error rate and the carrier-to-noise power ratio C/N which occurs in a prior-art 8PSK (8 or octonary phase shift keying) system. As shown in Fig. 28, the bit error rate (the curve A2) provided in the embodiment of this invention is better than that in the prior-art 8PSK system.

The inter-signal-point distance "$\sqrt{2p}$" in the QPSK modulation may be equal to "$\sqrt{2}$" times the inter-signal-point distance "2r" in the 16-value QAM. In this case, it is preferable that the quasi synchronous detector in the receiver detects the I-Q-plane amplitude of the output I and Q signals of the RF portion when the output I and Q signals of the RF portion 22 represent a pilot symbol, and that the detected I-Q-plane amplitude is used as an I-Q-plane amplitude threshold value for the 16-value QAM demodulation.

Fourteenth Embodiment

A fourteenth embodiment of this invention is similar to the tenth embodiment thereof except for design changes indicated hereinafter.

A pair of the I signal and the Q signal outputted from the

quadrature baseband modulator in the transmitter (see Fig. 1), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, first alternate symbols result from the QPSK modulation, and second alternate symbols result from the 16-value QAM. The QPSK symbols in every frame are used by the receiver as pilot symbols for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 3), the calculator 25 separates pilot symbols from the output I and Q signals of the RF portion 22 in response to a signal (a 2-symbol sync signal) having a period corresponding to two symbols. The calculator 25 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 26 separates pilot symbols from the output I and Q signals of the RF portion 22 in response to a signal (a 2-symbol sync signal) having a period corresponding to 2 symbols. The calculator 26 estimates a frequency offset amount from the separated pilot symbols.

Preferably, the maximum amplitude provided by the 16-value QAM, that is, the value given by the expression (10), is equal to the amplitude "p" provided by the QPSK modulation. In this case, the amplitude distortion amount and the frequency offset amount can be accurately estimated.

The quasi synchronous detector 29 in the receiver (see Fig. 3)

is designed to implement the following processes. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a pilot symbol. The quasi synchronous detector 29 subjects the output I and Q signals of the RF portion 22 to 16-value QAM demodulation and the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 22 represent a normal symbol different from a pilot symbol.

In general, the inter-signal-point distance "$\sqrt{2}p$" in the QPSK modulation is equal to a given value times the inter-signal-point distance "2r" in the 16-value QAM. Preferably, the given value is in the range of 0.90 to 1.50. In this case, a sufficiently low bit error rate is provided.

With reference to Fig. 29, in the case where the inter-signal-point distance "$\sqrt{2}p$" in the QPSK modulation is equal to 1.20 times the inter-signal-point distance "2r" in the 16-value QAM, the bit error rate provided in the embodiment of this invention decreases along the curve A3 as the carrier-to-noise power ratio C/N increases. Fig. 29 also indicates a comparative example being the relation B3 between the bit error rate and the carrier-to-noise power ratio C/N which occurs in a prior-art 8PSK (8 or octonary phase shift keying) system. As shown in Fig. 29, the bit error rate (the curve A3) provided in the embodiment of this invention is better than that in the prior-art 8PSK system.

The inter-signal-point distance "$\sqrt{2}p$" in the QPSK modulation may be equal to twice the inter-signal-point distance "2r" in the 16-value QAM. In this case, it is preferable that the quasi synchronous detector in the receiver detects the I-Q-plane amplitude of the output I and Q signals of the RF portion when the output I and Q signals of the RF portion 22 represent a pilot symbol, and that the detected I-Q-plane amplitude is used as an I-Q-plane amplitude threshold value for the 16-value QAM demodulation.

Fifteenth Embodiment

Fig. 30 shows a transmitter 110 in a radio communication system according to a fifteenth embodiment of this invention. With reference to Fig. 30, the transmitter 110 includes a modulator (a quadrature baseband modulator) 112 and an RF (radio frequency) portion 115.

A digital signal to be transmitted (that is, an input digital signal or main information to be transmitted) is fed to the quadrature baseband modulator 112. The device 112 subjects the input digital signal to quadrature baseband modulation, thereby converting the input digital signal into a pair of modulation-resultant baseband signals, that is, a baseband I (in-phase) signal and a baseband Q (quadrature) signal. The quadrature baseband modulator 112 outputs the baseband I signal and the baseband Q signal to the RF portion 115.

The RF portion 115 converts the baseband I signal and the baseband Q signal into an RF signal through frequency conversion. The RF portion 115 feeds the RF signal to an antenna 117. The RF

signal is radiated by the antenna 117.

As shown in Fig. 31, the quadrature baseband modulator 112 includes a 8PSK (8 or octonary phase shift keying) modulator 112A, a BPSK (binary phase shift keying) modulator 112B, a reference signal generator 112C, and switches 112D and 112E.

The 8PSK modulator 112A and the BPSK modulator 112B receives the input digital signal. The device 112A subjects the input digital signal to 8PSK (8PSK modulation), thereby converting the input digital signal into a pair of a baseband I signal and a baseband Q signal. The 8PSK modulator 112A outputs the baseband I signal to the switch 112D. The 8PSK modulator 112A outputs the baseband Q signal to the switch 112E. The device 112B subjects the input digital signal to BPSK (BPSK modulation), thereby converting the input digital signal into a pair of a baseband I signal and a baseband Q signal. The BPSK modulator 112B outputs the baseband I signal to the switch 112D. The BPSK modulator 112B outputs the baseband Q signal to the switch 112E. The reference signal generator 112C outputs a reference baseband I signal to the switch 112D. The reference signal generator 112C outputs a reference baseband Q signal to the switch 112E. The output I and Q signals from the reference signal generator 112C are used in acquiring synchronization between the transmitter 110 and a receiver during an initial stage of signal transmission. The switch 112D selects one of the output I signal from the 8PSK modulator 112A, the output I signal from the BPSK modulator 112B, and the output I signal from the reference signal generator 112C, and transmits the selected I

modulator 112B.

Fig. 32 shows a receiver 120 in the radio communication system according to the fifteenth embodiment of this invention. With reference to Fig. 32, the receiver 120 includes an RF portion 122, calculators 125 and 126, and a quasi synchronous detector 129.

An RF signal caught by an antenna 121 is applied to the RF portion 122. The RF portion 122 subjects the applied RF signal to frequency conversion, thereby converting the applied RF signal into a pair of a baseband I signal and a baseband Q signal. The RF portion 122 outputs the baseband I signal and the baseband Q signal to the calculators 125 and 126, and the quasi synchronous detector 129.

The calculator 125 estimates an amplitude distortion amount from the baseband I signal and the baseband Q signal. The calculator 125 informs the quasi synchronous detector 129 of the estimated amplitude distortion amount. The calculator 126 estimates a frequency offset amount from the baseband I signal and the baseband Q signal. The calculator 126 informs the quasi synchronous detector 129 of the estimated frequency offset amount.

The device 129 subjects the baseband I signal and the baseband Q signal to quasi synchronous detection responsive to the estimated amplitude distortion amount and the estimated frequency offset amount, thereby demodulating the baseband I signal and the baseband Q signal into an original digital signal. Thus, the quasi synchronous detector 129 recovers the original digital signal from the baseband I signal and the baseband Q signal. The quasi

synchronous detector 129 outputs the recovered original digital signal.

As shown in Fig. 33, the quasi synchronous detector 129 includes an 8PSK demodulator 129A, a BPSK demodulator 129B, and a switch 129C.

The 8PSK demodulator 129A and the BPSK demodulator 129B receive the output I and Q signals from the RF portion 122. In addition, the 8PSK demodulator 129A and the BPSK demodulator 129B are informed of the estimated amplitude distortion amount and the estimated frequency offset amount by the calculators 125 and 126.

The device 129A subjects the baseband I signal and the baseband Q signal to 8PSK demodulation responsive to the estimated amplitude distortion amount and the estimated frequency offset amount, thereby demodulating the baseband I signal and the baseband Q signal into an original digital signal. Thus, the 8PSK demodulator 129A recovers the original digital signal from the baseband I signal and the baseband Q signal. The 8PSK demodulator 129A outputs the recovered original digital signal to the switch 129C.

The device 129B subjects the baseband I signal and the baseband Q signal to BPSK demodulation responsive to the estimated amplitude distortion amount and the estimated frequency offset amount, thereby demodulating the baseband I signal and the baseband Q signal into an original digital signal. Thus, the BPSK demodulator 129B recovers the original digital signal from the

baseband I signal and the baseband Q signal. The BPSK demodulator 129B outputs the recovered original digital signal to the switch 129C.

The switch 129C alternately selects the output digital signal from the 8PSK demodulator 129A and the output digital signal from the BPSK demodulator 129B in response to a timing signal (a frame and symbol sync signal), and transmits the selected digital signal to a later stage. When the baseband I and Q signals outputted from the RF portion 122 to the quasi synchronous detector 129 correspond to a result of the 8PSK modulation, the switch 129C selects the output digital signal from the 8PSK demodulator 129A. When the baseband I and Q signals outputted from the RF portion 122 to the quasi synchronous detector 129 correspond to a result of the BPSK modulation, the switch 129C selects the output digital signal from the BPSK demodulator 129B.

For example, the 8PSK demodulator 129A includes an amplitude correction circuit and a frequency correction circuit. The amplitude correction circuit compensates for an amplitude distortion of the baseband I signal and the baseband Q signal in response to the estimated amplitude distortion, thereby generating a first compensation-resultant baseband I signal and a first compensation-resultant baseband Q signal. The frequency correction circuit compensates for a frequency offset of the first compensation-resultant baseband I signal and the first compensation-resultant baseband Q signal in response to the estimated frequency offset amount, thereby generating a second

compensation-resultant baseband I signal and a second compensation-resultant baseband Q signal. In the 8PSK demodulator 129A, the second compensation-resultant baseband I signal and the second compensation-resultant baseband Q signal are subjected to the 8PSK demodulation, being converted into the original digital signal.

For example, the BPSK demodulator 129B includes an amplitude correction circuit and a frequency correction circuit. The amplitude correction circuit compensates for an amplitude distortion of the baseband I signal and the baseband Q signal in response to the estimated amplitude distortion, thereby generating a first compensation-resultant baseband I signal and a first compensation-resultant baseband Q signal. The frequency correction circuit compensates for a frequency offset of the first compensation-resultant baseband I signal and the first compensation-resultant baseband Q signal in response to the estimated frequency offset amount, thereby generating a second compensation-resultant baseband I signal and a second compensation-resultant baseband Q signal. In the BPSK demodulator 129B, the second compensation-resultant baseband I signal and the second compensation-resultant baseband Q signal are subjected to the BPSK demodulation, being converted into the original digital signal.

Fig. 34 shows an arrangement of 8 signal points in an I-Q plane which are provided by the 8PSK modulation. In Fig. 34, the 8 signal points are denoted by the reference numeral "101A". The 8

signal points are assigned to 8 different levels (8 different logic states) respectively. The positions (I_{8PSK}, Q_{8PSK}) of the 8 signal points are given by the following equations.

$$I_{8PSK} = p \cdot \cos(\frac{k\pi}{4}) \quad \cdots(17)$$

$$Q_{8PSK} = p \cdot \sin(\frac{k\pi}{4}) \quad \cdots(18)$$

where "k" denotes a variable integer, and "p" denotes a predetermined constant.

Fig. 35 shows an arrangement of two signal points in an I-Q plane which are provided by the BPSK modulation. In Fig. 35, the signal points are denoted by the reference numeral "201A". The positions (I_{BPSK}, Q_{BPSK}) of the signal points are given by the following equations.

$$I_{BPSK} = q \cdot \cos(k\pi) \quad \cdots(19)$$

$$Q_{BPSK} = q \cdot \sin(k\pi) \quad \cdots(20)$$

where "k" denotes a variable integer, and "q" denotes a predetermined constant. With reference to Fig. 35, the signal points are on the I axis, and correspond to a same amplitude given by the constant "q". In addition, the signal points are spaced at an angle of π radian. Accordingly, a BPSK modulation-resultant signal is suited for detecting an amplitude distortion and a frequency offset.

With reference to Fig. 36, a pair of the I signal and the Q signal outputted from the quadrature baseband modulator 112 in the transmitter 110, or the RF signal outputted from the RF portion 115 in the transmitter 110 is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined

natural number. In every frame, the first symbol results from the BPSK modulation, and the second and later symbols result from the 8PSK modulation. The first symbol in every frame (that is, the BPSK symbol in every frame) is used by the receiver 120 as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver 120, the calculator 125 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 125 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 126 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 126 estimates a frequency offset amount from the separated pilot symbols.

The quasi synchronous detector 129 in the receiver 120 is designed to implement the following processes. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to the BPSK demodulation and outputs the BPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a pilot symbol. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to the 8PSK demodulation and outputs the 8PSK-

demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a normal symbol different from a pilot symbol.

The BPSK modulator 112B in the quadrature baseband modulator 112 of the transmitter 110 is designed to implement processes indicated below. The phase of an i-th BPSK symbol in the I-Q plane is denoted by "ϕ_i", and the phase of an (i+1)-th BPSK symbol in the I-Q plane is denoted by "ϕ_{i+1}". The BPSK modulator 112B determines the phase "θ_{i+1}" of the (i+1)-th BPSK symbol in an x-y plane on the basis of the difference between the phases "ϕ_i" and "ϕ_{i+1}" according to the following equation.

$$\theta_{i+1} = \phi_{i+1} - \phi_i \quad (\text{mod. } 2\pi) \qquad \cdots(21)$$

The BPSK modulator 112B implements BPSK modulation providing two signal points which are respectively on the positive side and the negative side of the x axis in the x-y plane as shown in Fig. 37. The BPSK modulator 112B assigns a bit of "0" and a bit of "1" in the input digital signal to the positive signal point and the negative signal point, respectively. Accordingly, a bit of "0" corresponds to the absence of a phase change of π radian between two successively symbols while a bit of "1" corresponds to the presence of a phase change of π radian between two successively symbols as in differential phase shift keying (DPSK). The BPSK modulator 112B outputs a pair of modulation-resultant I and Q signals to the switches 112D and 112E. The BPSK modulator 112B includes a latch or a register for sampling and holding a pair of modulation-resultant I and Q signals which are selected by the switches 112D

and 112E. The modulation-resultant I and Q signals held by the latch or the register are periodically updated. The BPSK modulator 112B outputs a pair of held modulation-resultant I and Q signals to the 8PSK modulator 112A.

As previously indicated, the 8PSK modulation implemented by the 8PSK modulator 112A provides 8 different signal points to which 8 different logic states are assigned respectively. For symbols following a BPSK symbol in every frame, the 8PSK modulator 112A determines the assignment of the logic states to the signal points on the basis of the signal point used by the BPSK symbol. The signal point used by the BPSK symbol is represented by a pair of BPSK-modulation-resultant I and Q signals fed from the BPSK modulator 112B. In the case where a signal point 501 on the positive side of the I axis is used by a BPSK symbol, the 8PSK modulator 112A assigns 3-bit sets of "000", "001", "010", "011", "100", "101", "110", and "111" in the input digital signal to eight signal points 502 for following symbols as shown in Fig. 38. In the case where a signal point 501 on the negative side of the I axis is used by a BPSK symbol, the 8PSK modulator 112A assigns 3-bit sets of "000", "001", "010", "011", "100", "101", "110", and "111" in the input digital signal to eight signal points 502 for following symbols as shown in Fig. 39.

Sixteenth Embodiment

A sixteenth embodiment of this invention is similar to the fifteenth embodiment thereof except for design changes indicated hereinafter.

As shown in Fig. 40, a modulator (a quadrature baseband modulator) in a transmitter in the sixteenth embodiment of this invention includes a 2^{2m}-value QAM (quadrature amplitude modulation) modulator 112F instead of the 8PSK modulator 112A (see Fig. 31). Here, "m" denotes a predetermined integer equal to or greater than "2".

As shown in Fig. 41, a quasi synchronous detector in a receiver in the sixteenth embodiment of this invention includes a 2^{2m}-value QAM demodulator 129D instead of the 8PSK demodulator 129A (see Fig. 33). The 2^{2m}-value QAM demodulator 129D implements demodulation inverse with respect to the modulation by the QAM modulator 112F.

Fig. 42 shows an arrangement of signal points in an I-Q plane which are provided by 2^{2m}-value QAM executed in the QAM modulator 112F. In Fig. 42, the signal points are denoted by the reference numeral "601A". The signal points are assigned to different values (different logic states) respectively. The positions (I_{QAM}, Q_{QAM}) of the signal points are given by the following equations.

$$I_{QAM} = r(2^{m-1}a1 + 2^{m-2}a2 + \bullet\bullet\bullet + 2^{0}am) \quad \cdots(22)$$

$$Q_{QAM} = r(2^{m-1}b1 + 2^{m-2}b2 + \bullet\bullet\bullet + 2^{0}bm) \quad \cdots(23)$$

where "m" denotes a predetermined integer equal to or greater than "2"; (a1, b1), (a2, b2), ···, (am, bm) are binary code words of "1" and "−1"; and "r" denotes a predetermined constant.

An example of the 2^{2m}-value QAM executed in the QAM modulator 112F is 16-value QAM. Fig. 43 shows an arrangement of

signal points in an I-Q plane which are provided by the 16-value QAM. In Fig. 43, the signal points are denoted by the reference numeral "701". The signal points are assigned to different values (different logic states) respectively. The positions (I_{16QAM}, Q_{16QAM}) of the signal points are given by the following equations.

$$I_{16QAM} = s(2^1a1 + 2^0a2) \quad \cdots(24)$$

$$Q_{16QAM} = s(2^1b1 + 2^0b2) \quad \cdots(25)$$

where (a1, b1) and (a2, b2) are binary code words of "1" and "−1", and "s" denotes a predetermined constant.

With reference to Fig. 44, a pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 30), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first symbol results from the BPSK modulation, and the second and later symbols result from the 16-value QAM. The first symbol in every frame (that is, the BPSK symbol in every frame) is used by the receiver as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 32), the calculator 125 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 125 estimates an amplitude distortion amount from the separated

pilot symbols. Similarly, the calculator 126 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 126 estimates a frequency offset amount from the separated pilot symbols.

The quasi synchronous detector 129 in the receiver (see Fig. 32) is designed to implement the following processes. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to BPSK demodulation and outputs the BPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a pilot symbol. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to 16-value QAM demodulation and outputs the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a normal symbol different from a pilot symbol.

The 16-value QAM implemented by the 16-value QAM modulator 112A provides 16 different signal points to which 16 different logic states are assigned respectively. For symbols following a BPSK symbol in every frame, the 16-value QAM modulator 112A determines the assignment of the logic stages to the signal points on the basis of the signal point used by the BPSK symbol. The signal point used by the BPSK symbol is represented by a pair of BPSK-modulation-resultant I and Q signals fed from the BPSK modulator 112B. In the case where a signal point 901A on

the positive side of the I axis is used by a BPSK symbol, the 16-value QAM modulator 112A assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to 16 signal points 902 for following symbols as shown in Fig. 45. In the case where a signal point 901A on the negative side of the I axis is used by a BPSK symbol, the 16-value QAM modulator 112A assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to 16 signal points 902 for following symbols as shown in Fig. 46.

Seventeenth Embodiment

A seventeenth embodiment of this invention is similar to the fifteenth embodiment thereof except for design changes indicated hereinafter.

As shown in Fig. 47, a modulator (a quadrature baseband modulator) in a transmitter in the seventeenth embodiment of this invention includes a 2^{2m}-value QAM (quadrature amplitude modulation) modulator 112G instead of the 8PSK modulator 112A (see Fig. 31). Here, "m" denotes a predetermined integer equal to or greater than "2".

As shown in Fig. 48, a quasi synchronous detector in a receiver in the seventeenth embodiment of this invention includes a 2^{2m}-value QAM demodulator 129E instead of the 8PSK demodulator 129A (see Fig. 33). The 2^{2m}-value QAM demodulator 129E implements demodulation inverse with respect to the modulation by the QAM modulator 112G.

Fig. 49 shows an arrangement of signal points in an I-Q plane

which are provided by 2^{2m}-value QAM executed in the QAM modulator 112G. In Fig. 49, the signal points are denoted by the reference numeral "1001A". The signal points are assigned to different logic values respectively. The positions of the signal points in Fig. 49 result from rotation of the signal points in Fig. 42 through an angle of $\pi/4$ radian about the origin. Specifically, the positions (I_{QAMR}, Q_{QAMR}) of the signal points in Fig. 49 are given by the following equations.

$$I_{QAMR} = I_{QAM}\{\cos(\frac{\pi}{4} + \frac{n\pi}{2})\} - Q_{QAM}\{\sin(\frac{\pi}{4} + \frac{n\pi}{2})\} \quad \cdots(26)$$

$$Q_{QAMR} = I_{QAM}\{\sin(\frac{\pi}{4} + \frac{n\pi}{2})\} + Q_{QAM}\{\cos(\frac{\pi}{4} + \frac{n\pi}{2})\} \quad \cdots(27)$$

where "n" denotes an integer, and (I_{QAM}, Q_{QAM}) are given by the equations (22) and (23).

An example of the 2^{2m}-value QAM executed in the QAM modulator 112G is 16-value QAM. Fig. 50 shows an arrangement of signal points in an I-Q plane which are provided by the 16-value QAM. In Fig. 50, the signal points are denoted by the reference numeral "1101". The signal points are assigned to different logic states (different values) respectively. The positions of the signal points in Fig. 50 result from rotation of the signal points in Fig. 43 through an angle of $\pi/4$ radian about the origin. Specifically, the positions (I_{16QAMR}, Q_{16QAMR}) of the signal points in Fig. 50 are given by the following equations.

$$I_{16QAMR} = I_{16QAM}\{\cos(\frac{\pi}{4} + \frac{n\pi}{2})\} - Q_{16QAM}\{\sin(\frac{\pi}{4} + \frac{n\pi}{2})\} \quad \cdots(28)$$

$$Q_{16QAMR} = I_{16QAM}\{\sin(\frac{\pi}{4} + \frac{n\pi}{2})\} + Q_{16QAM}\{\cos(\frac{\pi}{4} + \frac{n\pi}{2})\} \quad \cdots(29)$$

where "n" denotes an integer, and (I_{16QAM}, Q_{16QAM}) are given by the equations (24) and (25).

A pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 30), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first symbol results from the BPSK modulation, and the second and later symbols result from the 16-value QAM. The first symbol in every frame (that is, the BPSK symbol in every frame) is used by the receiver as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 32), the calculator 125 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 125 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 126 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 126 estimates a frequency offset amount from the separated pilot symbols.

The quasi synchronous detector 129 in the receiver (see Fig.

32) is designed to implement the following processes. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to BPSK demodulation and outputs the BPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a pilot symbol. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to 16-value QAM demodulation and outputs the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a normal symbol different from a pilot symbol.

The 16-value QAM implemented by the 16-value QAM modulator 112G provides 16 different signal points to which 16 different logic states are assigned respectively. For symbols following a BPSK symbol in every frame, the 16-value QAM modulator 112G determines the assignment of the logic states to the signal points on the basis of the signal point used by the BPSK symbol. The signal point used by the BPSK symbol is represented by a pair of BPSK-modulation-resultant I and Q signals fed from the BPSK modulator 112B. In the case where a signal point 1201 on the positive side of the I axis is used by a BPSK symbol, the 16-value QAM modulator 112G assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to 16 signal points 1202 for following symbols as shown in Fig. 51. In the case where a signal point 1201 on the negative side of the I axis is used by a BPSK symbol, the 16-value QAM modulator 112G assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input

digital signal to 16 signal points 1202 for following symbols as shown in Fig. 52.

Eighteenth Embodiment

An eighteenth embodiment of this invention is similar to the fifteenth embodiment thereof except for design changes indicated hereinafter.

As shown in Fig. 53, a modulator (a quadrature baseband modulator) in a transmitter in the eighteenth embodiment of this invention includes a QPSK (quadrature phase shift keying) modulator 112H instead of the BPSK modulator 112B (see Fig. 31).

As shown in Fig. 54, a quasi synchronous detector in a receiver in the eighteenth embodiment of this invention includes a QPSK demodulator 129F instead of the BPSK demodulator 129B (see Fig. 33). The QPSK demodulator 129F implements demodulation inverse with respect to the modulation by the QPSK modulator 112H.

Fig. 55 shows an arrangement of signal points in an I-Q plane which are provided by the QPSK modulation executed in the QPSK modulator 112H. In Fig. 55, the signal points are denoted by the reference numeral "1301". The positions (I_{QPSK}, Q_{QPSK}) of the signal points are given by the following equations.

$$I_{QPSK} = u\{\cos(\frac{\pi}{4})\cos(\frac{k\pi}{2}) - \sin(\frac{\pi}{4})\sin(\frac{k\pi}{2})\} \quad \cdots(30)$$

$$Q_{QPSK} = u\{\cos(\frac{\pi}{4})\sin(\frac{k\pi}{2}) + \sin(\frac{\pi}{4})\cos(\frac{k\pi}{2})\} \quad \cdots(31)$$

where "k" denotes a variable integer, and "u" denotes a predetermined constant. With reference to Fig. 55, all the signal

points correspond to a same amplitude given by the constant "u". In addition, all the distances between the neighboring signal points are equal to a same value given by $\sqrt{2u}$. Furthermore, the signal points are spaced at equal angular intervals. Accordingly, a QPSK modulation-resultant signal is suited for detecting an amplitude distortion and a frequency offset.

With reference to Fig. 56, a pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 30), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first symbol results from the QPSK modulation, and the second and later symbols result from the 8PSK modulation. The first symbol in every frame (that is, the QPSK symbol in every frame) is used by the receiver (see Fig. 32) as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 32), the calculator 125 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 125 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 126 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal)

having a period corresponding to N symbols. The calculator 126 estimates a frequency offset amount from the separated pilot symbols.

The quasi synchronous detector 129 in the receiver (see Fig. 32) is designed to implement the following processes. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a pilot symbol. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to 8PSK demodulation and outputs the 8PSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a normal symbol different from a pilot symbol.

The QPSK modulator 112H in the quadrature baseband modulator 112 of the transmitter is designed to implement processes indicated below. The phase of an i-th QPSK symbol in the I-Q plane is denoted by "ϕ_i", and the phase of an (i+1)-th QPSK symbol in the I-Q plane is denoted by "ϕ_{i+1}". The QPSK modulator 112H determines the phase "θ_{i+1}" of the (i+1)-th QPSK symbol in an x-y plane on the basis of the difference between the phases "ϕ_i" and "ϕ_{i+1}" according to the following equation.

$$\theta_{i+1} = \phi_{i+1} - \phi_i \quad (\text{mod. } 2\pi) \qquad \cdots(32)$$

The QPSK modulator 112H implements QPSK modulation providing four signal points which are respectively on the positive side of the x axis, the negative side of the x axis, the positive side of the y axis,

and the negative side of the y axis in the x-y plane as shown in Fig. 57. The QPSK modulator 112H assigns 2-bit sets of "00", "01", "10", and "11" to the positive-x signal point, the positive-y signal point, the negative-y signal point, and the negative-x signal point, respectively. Accordingly, a 2-bit set of "00" corresponds to the absence of any phase change between two successive symbols. A 2-bit set of "01" corresponds to the presence of a phase change of $\pi/2$ radian between two successive symbols. A 2-bit set of "11" corresponds to the presence of a phase change of π radian between two successive symbols. A 2-bit set of "10" corresponds to the presence of a phase change of $3\pi/2$ radian between two successive symbols. The QPSK modulator 112H outputs a pair of modulation-resultant I and Q signals to the switches 112D and 112E. The QPSK modulator 112H includes a latch or a register for sampling and holding a pair of modulation-resultant I and Q signals which are selected by the switches 112D and 112E. The modulation-resultant I and Q signals held by the latch or the register are periodically updated. The QPSK modulator 112H outputs a pair of held modulation-resultant I and Q signals to the 8PSK modulator 112A.

The 8PSK modulation implemented by the 8PSK modulator 112A provides 8 different signal points to which 8 different logic states are assigned respectively. For symbols following a QPSK symbol in every frame, the 8PSK modulator 112A determines the assignment of the logic states to the signal points on the basis of the signal point used by the QPSK symbol. The signal point used by the QPSK symbol is represented by a pair of QPSK-modulation-resultant

I and Q signals fed from the QPSK modulator 112H. In the case where a positive-I positive-Q signal point 1601 is used by a QPSK symbol, the 8PSK modulator 112A assigns 3-bit sets of "000", "001", "010", "011", "100", "101", "110", and "111" in the input digital signal to eight signal points 1602 for following symbols as shown in Fig. 58. In the case where a negative-I positive-Q signal point 1601 is used by a QPSK symbol, the 8PSK modulator 112A assigns 3-bit sets of "000", "001", "010", "011", "100", "101", "110", and "111" in the input digital signal to eight signal points 1602 for following symbols as shown in Fig. 59. In the case where a negative-I negative-Q signal point 1601 is used by a QPSK symbol, the 8PSK modulator 112A assigns 3-bit sets of "000", "001", "010", "011", "100", "101", "110", and "111" in the input digital signal to eight signal points 1602 for following symbols as shown in Fig. 60. In the case where a positive-I negative-Q signal point 1601 is used by a QPSK symbol, the 8PSK modulator 112A assigns 3-bit sets of "000", "001", "010", "011", "100", "101", "110", and "111" in the input digital signal to eight signal points 1602 for following symbols as shown in Fig. 61.

Nineteenth Embodiment

A nineteenth embodiment of this invention is similar to the sixteenth embodiment thereof except for design changes indicated hereinafter.

As shown in Fig. 62, a modulator (a quadrature baseband modulator) in a transmitter in the nineteenth embodiment of this invention includes a QPSK modulator 112H instead of the BPSK

modulator 112B (see Fig. 40).

As shown in Fig. 63, a quasi synchronous detector in a receiver in the nineteenth embodiment of this invention includes a QPSK demodulator 129F instead of the BPSK demodulator 129B (see Fig. 41). The QPSK demodulator 129F implements demodulation inverse with respect to the modulation by the QPSK modulator 112H.

The QPSK modulator 112H implements QPSK modulation providing signal points which are arranged in an I-Q plane as shown in Fig. 55. The positions (I_{QPSK}, Q_{QPSK}) of the signal points are given by the equations (30) and (31).

With reference to Fig. 64, a pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 30), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first symbol results from the QPSK modulation, and the second and later symbols result from the 2^{2m}-value QAM, for example, the 16-value QAM. The first symbol in every frame (that is, the QPSK symbol in every frame) is used by the receiver (see Fig. 32) as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 32), the calculator 125 separates pilot symbols (first symbols in frames) from the output I and Q signals of

the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 125 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 126 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 126 estimates a frequency offset amount from the separated pilot symbols.

The quasi synchronous detector 129 in the receiver (see Fig. 32) is designed to implement the following processes. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a pilot symbol. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to 2^{2m}-value QAM demodulation and outputs the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a normal symbol different from a pilot symbol.

The QPSK modulator 112H in the quadrature baseband modulator 112 of the transmitter is designed to implement processes indicated below. The phase of an i-th QPSK symbol in the I-Q plane is denoted by "ϕ_i", and the phase of an (i+1)-th QPSK symbol in the I-Q plane is denoted by "ϕ_{i+1}". The QPSK modulator 112H determines the phase "θ_{i+1}" of the (i+1)-th QPSK symbol in

an x-y plane on the basis of the difference between the phases "ϕ_i" and "ϕ_{i+1}" according to the equation (32). The QPSK modulator 112H implements QPSK modulation providing four signal points which are respectively on the positive side of the x axis, the negative side of the x axis, the positive side of the y axis, and the negative side of the y axis in the x-y plane as shown in Fig. 57. The QPSK modulator 112H assigns 2-bit sets of "00", "01", "10", and "11" to the positive-x signal point, the positive-y signal point, the negative-y signal point, and the negative-x signal point, respectively. The QPSK modulator 112H outputs a pair of modulation-resultant I and Q signals to the switches 112D and 112E. The QPSK modulator 112H includes a latch or a register for sampling and holding a pair of modulation-resultant I and Q signals which are selected by the switches 112D and 112E. The modulation-resultant I and Q signals held by the latch or the register are periodically updated. The QPSK modulator 112H outputs a pair of held modulation-resultant I and Q signals to the 2^{2m}-value QAM modulator 112F.

An example of the modulation implemented by the 2^{2m}-value QAM modulator 112F is the 16-value QAM. The 16-value QAM by the 2^{2m}-value QAM modulator 112F provides 16 different signal points to which 16 different logic states are assigned respectively. For symbols following a QPSK symbol in every frame, the 16-value QAM modulator 112F determines the assignment of the logic states to the signal points on the basis of the signal point used by the QPSK symbol. The signal point used by the QPSK symbol is represented by a pair of QPSK-modulation-resultant I and Q signals fed from the

QPSK modulator 112H. In the case where a positive-I positive-Q signal point 1801 is used by a QPSK symbol, the 16-value QAM modulator 112F assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to sixteen signal points 1802 for following symbols as shown in Fig. 65. In the case where a negative-I positive-Q signal point 1801 is used by a QPSK symbol, the 16-value QAM modulator 112F assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to sixteen signal points 1802 for following symbols as shown in Fig. 66. In the case where a negative-I negative-Q signal point 1801 is used by a QPSK symbol, the 16-value QAM modulator 112F assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to sixteen signal points 1802 for following symbols as shown in Fig. 67. In the case where a positive-I negative-Q signal point 1801 is used by a QPSK symbol, the 16-value QAM modulator 112F assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to sixteen signal points 1802 for following symbols as shown in Fig. 68.

Twentieth Embodiment

A twentieth embodiment of this invention is similar to the fifteenth embodiment thereof except for design changes indicated hereinafter.

As shown in Fig. 69, a modulator (a quadrature baseband modulator) in a transmitter in the twentieth embodiment of this invention includes a QPSK (quadrature phase shift keying) modulator 112J instead of the BPSK modulator 112B (see Fig. 31).

As shown in Fig. 70, a quasi synchronous detector in a receiver in the twentieth embodiment of this invention includes a QPSK demodulator 129G instead of the BPSK demodulator 129B (see Fig. 33). The QPSK demodulator 129G implements demodulation inverse with respect to the modulation by the QPSK modulator 112J.

Fig. 71 shows an arrangement of signal points in an I-Q plane which are provided by QPSK modulation implemented by the QPSK modulator 112J. In Fig. 71, the signal points are denoted by the reference numeral "1901". The positions (I_{QPSKR}, Q_{QPSKR}) of the signal points are given by the following equations.

$$I_{QPSKR} = I_{QPSK}\{\cos(\frac{\pi}{4} + \frac{n\pi}{2})\} - Q_{QPSK}\{\sin(\frac{\pi}{4} + \frac{n\pi}{2})\} \quad \cdots(33)$$

$$Q_{QPSKR} = I_{QPSK}\{\sin(\frac{\pi}{4} + \frac{n\pi}{2})\} + Q_{QPSK}\{\cos(\frac{\pi}{4} + \frac{n\pi}{2})\} \quad \cdots(34)$$

where "n" denotes an integer, and (I_{QPSK}, Q_{QPSK}) are given by the equations (30) and (31). With reference to Fig. 71, all the signal points correspond to a same amplitude. In addition, all the distances between the neighboring signal points are equal to a same value. Furthermore, the signal points are spaced at equal angular intervals. Accordingly, a QPSK modulation-resultant signal is suited for detecting an amplitude distortion and a frequency offset.

A pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 30), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame,

the first symbol results from the QPSK modulation, and the second and later symbols result from the 8PSK modulation. The first symbol in every frame (that is, the QPSK symbol in every frame) is used by the receiver (see Fig. 32) as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 32), the calculator 125 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 125 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 126 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 126 estimates a frequency offset amount from the separated pilot symbols.

The quasi synchronous detector 129 in the receiver (see Fig. 32) is designed to implement the following processes. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a pilot symbol. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to 8PSK demodulation and outputs the 8PSK-

demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a normal symbol different from a pilot symbol.

The QPSK modulator 112J in the quadrature baseband modulator 112 of the transmitter is designed to implement processes indicated below. The phase of an i-th QPSK symbol in the I-Q plane is denoted by "ϕ_i", and the phase of an (i+1)-th QPSK symbol in the I-Q plane is denoted by "ϕ_{i+1}". The QPSK modulator 112J determines the phase "θ_{i+1}" of the (i+1)-th QPSK symbol in an x-y plane on the basis of the difference between the phases "ϕ_i" and "ϕ_{i+1}" according to the following equation.

$$\theta_{i+1} = \phi_{i+1} - \phi_i \quad (\text{mod. } 2\pi) \qquad \cdots(35)$$

The QPSK modulator 112J implements QPSK modulation providing four signal points which are spaced at equal angular intervals. The QPSK modulator 112J assigns 2-bit sets of "00", "01", "10", and "11" to the four signal points respectively. The QPSK modulator 112J outputs a pair of modulation-resultant I and Q signals to the switches 112D and 112E. The QPSK modulator 112J includes a latch or a register for sampling and holding a pair of modulation-resultant I and Q signals which are selected by the switches 112D and 112E. The modulation-resultant I and Q signals held by the latch or the register are periodically updated. The QPSK modulator 112J outputs a pair of held modulation-resultant I and Q signals to the 8PSK modulator 112A.

The 8PSK modulation implemented by the 8PSK modulator 112A provides 8 different signal points to which 8 different logic

states are assigned respectively. For symbols following a QPSK symbol in every frame, the 8PSK modulator 112A determines the assignment of the logic states to the signal points on the basis of the signal point used by the QPSK symbol. The signal point used by the QPSK symbol is represented by a pair of QPSK-modulation-resultant I and Q signals fed from the QPSK modulator 112J. In the case where a signal point 2001 on the positive side of the I axis is used by a QPSK symbol, the 8PSK modulator 112A assigns 3-bit sets of "000", "001", "010", "011", "100", "101", "110", and "111" in the input digital signal to eight signal points 2002 for following symbols as shown in Fig. 72. In the case where a signal point 2001 on the positive side of the Q axis is used by a QPSK symbol, the 8PSK modulator 112A assigns 3-bit sets of "000", "001", "010", "011", "100", "101", "110", and "111" in the input digital signal to eight signal points 2002 for following symbols as shown in Fig. 73. In the case where a signal point 2001 on the negative side of the I axis is used by a QPSK symbol, the 8PSK modulator 112A assigns 3-bit sets of "000", "001", "010", "011", "100", "101", "110", and "111" in the input digital signal to eight signal points 2002 for following symbols as shown in Fig. 74. In the case where a signal point 2001 on the negative side of the Q axis is used by a QPSK symbol, the 8PSK modulator 112A assigns 3-bit sets of "000", "001", "010", "011", "100", "101", "110", and "111" in the input digital signal to eight signal points 2002 for following symbols as shown in Fig. 75.

Twenty-First Embodiment

A twenty-first embodiment of this invention is similar to the

sixteenth embodiment thereof except for design changes indicated hereinafter.

As shown in Fig. 76, a modulator (a quadrature baseband modulator) in a transmitter in the twenty-first embodiment of this invention includes a QPSK (quadrature phase shift keying) modulator 112J instead of the BPSK modulator 112B (see Fig. 40). The QPSK modulator 112J implements QPSK modulation providing signal points which are arranged in an I-Q plane as shown in Fig. 71.

As shown in Fig. 77, a quasi synchronous detector in a receiver in the twenty-first embodiment of this invention includes a QPSK demodulator 129G instead of the BPSK demodulator 129B (see Fig. 41). The QPSK demodulator 129G implements demodulation inverse with respect to the modulation by the QPSK modulator 112J.

A pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 30), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first symbol results from the QPSK modulation, and the second and later symbols result from the 2^{2m}-value QAM modulation. The first symbol in every frame (that is, the QPSK symbol in every frame) is used by the receiver (see Fig. 32) as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 32), the calculator 125 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 125 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 126 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 126 estimates a frequency offset amount from the separated pilot symbols.

The quasi synchronous detector 129 in the receiver (see Fig. 32) is designed to implement the following processes. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a pilot symbol. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to 2^{2m}-value QAM demodulation and outputs the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a normal symbol different from a pilot symbol.

The QPSK modulator 112J in the quadrature baseband modulator 112 of the transmitter is designed to implement processes indicated below. The phase of an i-th QPSK symbol in the I-Q plane is denoted by "ϕ_i", and the phase of an (i+1)-th QPSK

symbol in the I-Q plane is denoted by "ϕ_{i+1}". The QPSK modulator 112J determines the phase "θ_{i+1}" of the (i+1)-th QPSK symbol in an x-y plane on the basis of the difference between the phases "ϕ_i" and "ϕ_{i+1}" according to the equation (35). The QPSK modulator 112J implements QPSK modulation providing four signal points which are spaced at equal angular intervals. The QPSK modulator 112J assigns 2-bit sets of "00", "01", "10", and "11" to four signal points in the x-y plane respectively. The QPSK modulator 112J outputs a pair of modulation-resultant I and Q signals to the switches 112D and 112E. The QPSK modulator 112J includes a latch or a register for sampling and holding a pair of modulation-resultant I and Q signals which are selected by the switches 112D and 112E. The modulation-resultant I and Q signals held by the latch or the register are periodically updated. The QPSK modulator 112J outputs a pair of held modulation-resultant I and Q signals to the 2^{2m}-value QAM modulator 112F.

An example of the modulation implemented by the 2^{2m}-value QAM modulator 112F is the 16-value QAM. The 16-value QAM by the 2^{2m}-value QAM modulator 112F provides 16 different signal points to which 16 different logic states are assigned respectively. For symbols following a QPSK symbol in every frame, the 16-value QAM modulator 112F determines the assignment of the logic states to the signal points on the basis of the signal point used by the QPSK symbol. The signal point used by the QPSK symbol is represented by a pair of QPSK-modulation-resultant I and Q signals fed from the QPSK modulator 112J. In the case where a signal point 2101 on

the positive side of the I axis is used by a QPSK symbol, the 16-value QAM modulator 112F assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to sixteen signal points 2102 for following symbols as shown in Fig. 78. In the case where a signal point 2101 on the positive side of the Q axis is used by a QPSK symbol, the 16-value QAM modulator 112F assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to sixteen signal points 2102 for following symbols as shown in Fig. 79. In the case where a signal point 2101 on the negative side of the I axis is used by a QPSK symbol, the 16-value QAM modulator 112F assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to sixteen signal points 2102 for following symbols as shown in Fig. 80. In the case where a signal point 2101 on the negative side of the Q axis is used by a QPSK symbol, the 16-value QAM modulator 112F assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to sixteen signal points 2102 for following symbols as shown in Fig. 81.

Sheet 2 of 2 Serial No. 08/250,745

Twenty-Second Embodiment

A twenty-second embodiment of this invention is similar to the seventeenth embodiment thereof except for design changes indicated hereinafter.

As shown in Fig. 82, a modulator (a quadrature baseband modulator) in a transmitter in the twenty-second embodiment of this invention includes a QPSK (quadrature phase shift keying) modulator 112H instead of the BPSK modulator 112B (see Fig. 47).

The QPSK modulator 112H implements QPSK modulation providing signal points which are arranged in an I-Q plane as shown in Fig. 55.

As shown in Fig. 83, a quasi synchronous detector in a receiver in the twenty-second embodiment of this invention includes a QPSK demodulator 129F instead of the BPSK demodulator 129B (see Fig. 48). The QPSK demodulator 129F implements demodulation inverse with respect to the modulation by the QPSK modulator 112H.

A pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 30), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first symbol results from the QPSK modulation, and the second and later symbols result from the 2^{2m}-value QAM modulation. The first symbol in every frame (that is, the QPSK symbol in every frame) is used by the receiver (see Fig. 32) as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 32), the calculator 125 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 125 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 126 separates pilot symbols

EP 0 525 732 A2

(first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 126 estimates a frequency offset amount from the separated pilot symbols.

The quasi synchronous detector 129 in the receiver (see Fig. 32) is designed to implement the following processes. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a pilot symbol. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to 2^{2m}-value QAM demodulation and outputs the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a normal symbol different from a pilot symbol.

The QPSK modulator 112H in the quadrature baseband modulator 112 of the transmitter is designed to implement processes indicated below. The phase of an i-th QPSK symbol in the I-Q plane is denoted by "ϕ_i", and the phase of an (i+1)-th QPSK symbol in the I-Q plane is denoted by "ϕ_{i+1}". The QPSK modulator 112H determines the phase "θ_{i+1}" of the (i+1)-th QPSK symbol in an x-y plane on the basis of the difference between the phases "ϕ_i" and "ϕ_{i+1}" according to the equation (32). The QPSK modulator 112H implements QPSK modulation providing four signal points which are spaced at equal angular intervals. The QPSK modulator

112H assigns 2-bit sets of "00", "01", "10", and "11" to four signal points in the x-y plane respectively. The QPSK modulator 112H outputs a pair of modulation-resultant I and Q signals to the switches 112D and 112E. The QPSK modulator 112H includes a latch or a register for sampling and holding a pair of modulation-resultant I and Q signals which are selected by the switches 112D and 112E. The modulation-resultant I and Q signals held by the latch or the register are periodically updated. The QPSK modulator 112H outputs a pair of held modulation-resultant I and Q signals to the 2^{2m}-value QAM modulator 112G.

An example of the modulation implemented by the 2^{2m}-value QAM modulator 112G is the 16-value QAM. The 16-value QAM by the 2^{2m}-value QAM modulator 112G provides 16 different signal points to which 16 different logic states are assigned respectively. For symbols following a QPSK symbol in every frame, the 16-value QAM modulator 112G determines the assignment of the logic states to the signal points on the basis of the signal point used by the QPSK symbol. The signal point used by the QPSK symbol is represented by a pair of QPSK-modulation-resultant I and Q signals fed from the QPSK modulator 112H. In the case where a positive-I positive-Q signal point 2201 is used by a QPSK symbol, the 16-value QAM modulator 112G assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to sixteen signal points 2202 for following symbols as shown in Fig. 84. In the case where a negative-I positive-Q signal point 2201 is used by a QPSK symbol, the 16-value QAM modulator 112G assigns 4-bit sets of

"0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to sixteen signal points 2202 for following symbols as shown in Fig. 85. In the case where a negative-I negative-Q signal point 2201 is used by a QPSK symbol, the 16-value QAM modulator 112G assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to sixteen signal points 2202 for following symbols as shown in Fig. 86. In the case where a positive-I negative-Q signal point 2201 is used by a QPSK symbol, the 16-value QAM modulator 112G assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to sixteen signal points 2202 for following symbols as shown in Fig. 87.

Twenty-Third Embodiment

A twenty-third embodiment of this invention is similar to the seventeenth embodiment thereof except for design changes indicated hereinafter.

As shown in Fig. 88, a modulator (a quadrature baseband modulator) in a transmitter in the twenty-third embodiment of this invention includes a QPSK (quadrature phase shift keying) modulator 112J instead of the BPSK modulator 112B (see Fig. 47). The QPSK modulator 112J implements QPSK modulation providing signal points which are arranged in an I-Q plane as shown in Fig. 71.

As shown in Fig. 89, a quasi synchronous detector in a receiver in the twenty-second embodiment of this invention includes a QPSK demodulator 129G instead of the BPSK demodulator 129B (see Fig. 48). The QPSK demodulator 129G implements demodulation inverse with respect to the modulation by

the QPSK modulator 112J.

A pair of the I signal and the Q signal outputted from the quadrature baseband modulator in the transmitter (see Fig. 30), or the RF signal outputted from the RF portion in the transmitter is composed of a stream of frames each having N successive symbols. Here, N denotes a predetermined natural number. In every frame, the first symbol results from the QPSK modulation, and the second and later symbols result from the 2^{2m}-value QAM modulation. The first symbol in every frame (that is, the QPSK symbol in every frame) is used by the receiver (see Fig. 32) as a pilot symbol for estimating an amplitude distortion amount and a frequency offset amount. It should be noted that every pilot symbol also carries a part of the main information to be transmitted.

In the receiver (see Fig. 32), the calculator 125 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 125 estimates an amplitude distortion amount from the separated pilot symbols. Similarly, the calculator 126 separates pilot symbols (first symbols in frames) from the output I and Q signals of the RF portion 122 in response to a signal (a frame and symbol sync signal) having a period corresponding to N symbols. The calculator 126 estimates a frequency offset amount from the separated pilot symbols.

The quasi synchronous detector 129 in the receiver (see Fig. 32) is designed to implement the following processes. The quasi

synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to QPSK demodulation and outputs the QPSK-demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a pilot symbol. The quasi synchronous detector 129 subjects the output I and Q signals of the RF portion 122 to 2^{2m}-value QAM demodulation and outputs the QAM-demodulation-resultant digital signal when the output I and Q signals of the RF portion 122 represent a normal symbol different from a pilot symbol.

The QPSK modulator 112J in the quadrature baseband modulator 112 of the transmitter is designed to implement processes indicated below. The phase of an i-th QPSK symbol in the I-Q plane is denoted by "ϕ_i", and the phase of an (i+1)-th QPSK symbol in the I-Q plane is denoted by "ϕ_{i+1}". The QPSK modulator 112H determines the phase "θ_{i+1}" of the (i+1)-th QPSK symbol in an x-y plane on the basis of the difference between the phases "ϕ_i" and "ϕ_{i+1}" according to the equation (35). The QPSK modulator 112J implements QPSK modulation providing four signal points which are spaced at equal angular intervals. The QPSK modulator 112J assigns 2-bit sets of "00", "01", "10", and "11" to four signal points in the x-y plane respectively. The QPSK modulator 112J outputs a pair of modulation-resultant I and Q signals to the switches 112D and 112E. The QPSK modulator 112J includes a latch or a register for sampling and holding a pair of modulation-resultant I and Q signals which are selected by the switches 112D and 112E. The modulation-resultant I and Q signals held by the

latch or the register are periodically updated. The QPSK modulator 112J outputs a pair of held modulation-resultant I and Q signals to the 2^{2m}-value QAM modulator 112G.

An example of the modulation implemented by the 2^{2m}-value QAM modulator 112G is the 16-value QAM. The 16-value QAM by the 2^{2m}-value QAM modulator 112G provides 16 different signal points to which 16 different logic states are assigned respectively. For symbols following a QPSK symbol in every frame, the 16-value QAM modulator 112G determines the assignment of the logic states to the signal points on the basis of the signal point used by the QPSK symbol. The signal point used by the QPSK symbol is represented by a pair of QPSK-modulation-resultant I and Q signals fed from the QPSK modulator 112J. In the case where a signal point 2301 on the positive side of the I axis is used by a QPSK symbol, the 16-value QAM modulator 112G assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to sixteen signal points 2302 for following symbols as shown in Fig. 90. In the case where a signal point 2301 on the positive side of the Q axis is used by a QPSK symbol, the 16-value QAM modulator 112G assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to sixteen signal points 2302 for following symbols as shown in Fig. 91. In the case where a signal point 2301 on the negative side of the I axis is used by a QPSK symbol, the 16-value QAM modulator 112G assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to sixteen signal points 2302 for following symbols as shown in Fig. 92. In the case

where a signal point 2301 on the negative side of the Q axis is used by a QPSK symbol, the 16-value QAM modulator 112G assigns 4-bit sets of "0000", "0001", "0010", ···, "1110", and "1111" in the input digital signal to sixteen signal points 2302 for following symbols as shown in Fig. 93.

Simulation

Simulation was executed by a computer. During the simulation, normal symbols were made on the basis of 16-value QAM while pilot symbols were made on the basis of QPSK modulation according to this invention. The normal symbols and the pilot symbols were combined into a symbol stream in a way based on this invention. In the symbol stream, the number of normal symbols between pilot symbols (that is, a data symbol length) was equal to a given natural number "n" while each of the separate pilot symbols was equal to "1" in length. The given natural number "n" was "1", "7", or "15". Accordingly, symbol streams of three types were generated. During the simulation, each of the first-type symbol stream, the second-type symbol stream, and the third-type symbol stream was transmitted from a transmitter to a receiver. In the receiver, normal symbols were subjected to quasi synchronous detection using 16-value QAM demodulation while pilot symbols were subjected to delayed detection using QPSK demodulation. Regarding the transmission of each of the first-type symbol stream, the second-type symbol stream, and the third-type symbol stream, the bit error rate was calculated at a varying ratio of the 1-bit signal energy "Eb" to the noise power density "N0". In the case where the

given natural number "n" was equal to "1", as the ratio of the 1-bit signal energy "Eb" to the noise power density "N0" increased, the calculated bit error rate decreased along the curve D1 of Fig. 94. In the case where the given natural number "n" was equal to "7", as the ratio of the 1-bit signal energy "Eb" to the noise power density "N0" increased, the calculated bit error rate decreased along the curve D7 of Fig. 94. In the case where the given natural number "n" was equal to "15", as the ratio of the 1-bit signal energy "Eb" to the noise power density "N0" increased, the calculated bit error rate decreased along the curve D15 of Fig. 94.

As comparative examples, similar simulation was implemented on a prior-art system. Specifically, normal symbols were made on the basis of 16-value QAM while a signal point corresponding to a maximum amplitude was used as pilot symbols. The normal symbols and the pilot symbols were combined into a symbol stream in a prior-art way. In the symbol stream, the number of normal symbols between pilot symbols (that is, a data symbol length) was equal to a given natural number "n" while each of the separate pilot symbols was equal to "1" in length. The given natural number "n" was "1", "7", or "15". Accordingly, symbol streams of three types were generated. Each of the first-type symbol stream, the second-type symbol stream, and the third-type symbol stream was transmitted from a transmitter to a receiver. In the receiver, the transmitted symbol stream was subjected to quasi synchronous detection using 16-value QAM demodulation. Regarding the transmission of each of the first-type symbol stream, the second-type symbol stream, and

the third-type symbol stream, the bit error rate was calculated at a varying ratio of the 1-bit signal energy "Eb" to the noise power density "N0". In the case where the given natural number "n" was equal to "1", as the ratio of the 1-bit signal energy "Eb" to the noise power density "N0" increased, the calculated bit error rate decreased along the curve E1 of Fig. 94. In the case where the given natural number "n" was equal to "7", as the ratio of the 1-bit signal energy "Eb" to the noise power density "N0" increased, the calculated bit error rate decreased along the curve E7 of Fig. 94. In the case where the given natural number "n" was equal to "15", as the ratio of the 1-bit signal energy "Eb" to the noise power density "N0" increased, the calculated bit error rate decreased along the curve E15 of Fig. 94.

As shown in Fig. 94, the bit error rates (the curves D1, D7, and D15) in this invention are better than the corresponding prior-art bit error rates (the curves E1, E7, and E15).

EP 0 525 968 A2

WHAT IS CLAIMED IS:

1. A method of modulation, comprising the steps of:

periodically and alternately subjecting an input digital signal to first modulation and second modulation to convert the input digital signal into a pair of a baseband I signal and a baseband Q signal, the first modulation and the second modulation being different from each other; and

outputting the pair of the baseband I signal and the baseband Q signal.

2. A method as recited in claim 1, wherein the first modulation is at least 8-signal-point modulation, and the second modulation is phase shift keying.

3. A method as recited in claim 2, wherein the phase shift keying is quadrature phase shift keying.

4. A method as recited in claim 3, wherein the quadrature phase shift keying provides signal points on an I axis and a Q axis in an I-Q plane.

5. A method as recited in claim 2, wherein the at least 8-signal-point modulation is at least 8 quadrature amplitude modulation.

6. A method as recited in claim 4, wherein the at least 8-signal-

point modulation is at least 8 quadrature amplitude modulation.

7. A method as recited in claim 5, wherein the at least 8 quadrature amplitude modulation is 16 quadrature amplitude modulation.

8. A method as recited in claim 6, wherein the at least 8 quadrature amplitude modulation is 16 quadrature amplitude modulation.

9. A method as recited in claim 5, wherein the at least 8 quadrature amplitude modulation provides signal points which result from rotation of signal points of at least 8-value normal quadrature amplitude modulation through an angle of $\pi/4$ radian about an origin in an I-Q plane.

10. A method as recited in claim 6, wherein the at least 8 quadrature amplitude modulation provides signal points which result from rotation of signal points of at least 8-value normal quadrature amplitude modulation through an angle of $\pi/4$ radian about an origin in an I-Q plane.

11. A method as recited in claim 7, wherein the 16 quadrature amplitude modulation provides signal points which result from rotation of signal points of 16-value normal quadrature amplitude modulation through an angle of $\pi/4$ radian about an origin in an I-Q

plane.

12. A method as recited in claim 8, wherein the 16 quadrature amplitude modulation provides signal points which result from rotation of signal points of 16-value normal quadrature amplitude modulation through an angle of $\pi/4$ radian about an origin in an I-Q plane.

13. A method as recited in claim 2, wherein a maximum of amplitudes corresponding to signal points of the at least 8-signal-point modulation in an I-Q plane is equal to an amplitude of a signal point of the phase shift keying in the I-Q plane.

14. A method as recited in claim 7, wherein a distance between signal points of the 16 quadrature amplitude modulation in an I-Q plane is equal to a given value times a distance between signal points of the phase shift keying in the I-Q plane, the given value being in a range of 0.9 to 1.5.

15. A method as recited in claim 7, wherein a distance between signal points of the 16 quadrature amplitude modulation in an I-Q plane is equal to twice a distance between signal points of the phase shift keying in the I-Q plane.

16. A method as recited in claim 8, wherein a distance between signal points of the 16 quadrature amplitude modulation in the I-Q

plane is equal to $\sqrt{2}$ times a distance between signal points of the quadrature phase shift keying in the I-Q plane.

17. A method as recited in claim 2, wherein the phase shift keying providing periodically-spaced symbols which represent corresponding portions of the input digital signal in terms of differences between phases of the periodically-spaced symbols.

18. A method as recited in claim 17, wherein the at least 8-signal-point modulation assigns logic states of the input digital signal to respective signal points for a first symbol in response to a signal point used by a second symbol of the phase shift keying which precedes the first symbol.

19. A method as recited in claim 17, wherein the at least 8-signal-point modulation is at least 8 quadrature amplitude modulation.

20. A method as recited in claim 19, wherein the at least 8 quadrature amplitude modulation is 16 quadrature amplitude modulation.

21. A method as recited in claim 19, wherein the at least 8 quadrature amplitude modulation provides signal points which result from rotation of signal points of at least 8-value normal quadrature amplitude modulation through an angle of $\pi/4$ radian about an origin in an I-Q plane.

22. A method as recited in claim 20, wherein the 16 quadrature amplitude modulation provides signal points which result from rotation of signal points of 16-value normal quadrature amplitude modulation through an angle of $\pi/4$ radian about an origin in an I-Q plane.

23. A method as recited in claim 17, wherein the phase shift keying is quadrature phase shift keying.

24. A method as recited in claim 23, wherein the quadrature phase shift keying provides signal points on an I axis and a Q axis in an I-Q plane.

25. A method as recited in claim 1, wherein the first modulation is 16 quadrature amplitude modulation, and the second modulation is quadrature phase shift keying.

26. A method as recited in claim 25, wherein the 16 quadrature amplitude modulation provides signal points which result from rotation of signal points of 16-value normal quadrature amplitude modulation through an angle of $\pi/4$ radian about an origin in an I-Q plane.

27. A method as recited in claim 25, wherein the quadrature phase shift keying provides signal points on an I axis and a Q axis in

an I-Q plane.

28. A method as recited in claim 25, wherein the 16 quadrature amplitude modulation provides signal points which result from rotation of signal points of 16-value normal quadrature amplitude modulation through an angle of $\pi/4$ radian about an origin in an I-Q plane, and the quadrature phase shift keying provides signal points on an I axis and a Q axis in the I-Q plane.

29. A method as recited in claim 25, wherein a maximum of amplitudes corresponding to signal points of the 16 quadrature amplitude modulation in an I-Q plane is equal to an amplitude of a signal point of the quadrature phase shift keying in the I-Q plane.

30. A method as recited in claim 25, wherein a distance between signal points of the 16 quadrature amplitude modulation in an I-Q plane is equal to a given value times a distance between signal points of the quadrature phase shift keying in the I-Q plane, the given value being in a range of 0.9 to 1.5.

31. A method as recited in claim 25, wherein a distance between signal points of the 16 quadrature amplitude modulation in an I-Q plane is equal to twice a distance between signal points of the quadrature phase shift keying in the I-Q plane.

32. A method as recited in claim 26, wherein a distance between

signal points of the 16 quadrature amplitude modulation in the I-Q plane is equal to $\sqrt{2}$ times a distance between signal points of the quadrature phase shift keying in the I-Q plane.

33. A transmission apparatus comprising:

first means for periodically and alternately subjecting an input digital signal to first modulation and second modulation to convert the input digital signal into a pair of a baseband I signal and a baseband Q signal, the first modulation and the second modulation being different from each other, the first modulation being at least 8-signal-point modulation, the second modulation being phase shift keying; and

second means for outputting the pair of the baseband I signal and the baseband Q signal.

34. A reception apparatus comprising:

first means for recovering a pair of a baseband I signal and a baseband Q signal from a received signal; and

second means for periodically and alternately subjecting the pair of the baseband I signal and the baseband Q signal to first demodulation and second demodulation to convert the pair of the baseband I signal and the baseband Q signal into an original digital signal;

wherein the first demodulation is for signals of at least 8 signal points modulation, and the second demodulation is phase shift keying demodulation.

0240242 - 020399

35. A radio communication system comprising:

a transmission apparatus including:

a1) first means for periodically and alternately subjecting an input digital signal to first modulation and second modulation to convert the input digital signal into a pair of a baseband I signal and a baseband Q signal, the first modulation and the second modulation being different from each other, the first modulation being at least 8-signal-point modulation, the second modulation being phase shift keying;

a2) second means for converting the pair of the baseband I signal and the baseband Q signal generated by the first means into a corresponding RF signal; and

a3) third means for transmitting the RF signal generated by the second means;

a reception apparatus including:

b1) fourth means for receiving the RF signal transmitted by the third means;

b2) fifth means for recovering a pair of a baseband I signal and a baseband Q signal from the RF signal received by the fourth means; and

b3) sixth means for periodically and alternately subjecting the pair of the baseband I signal and the baseband Q signal recovered by the fifth means to first demodulation and second demodulation to convert the pair of the baseband I signal and the baseband Q signal into an original digital signal;

wherein the first demodulation is for signals of at least 8 signal points modulation, and the second demodulation is phase shift keying demodulation.

Page 3 of 3 - 9/26/2006 3:35:05 PM

ABSTRACT OF THE DISCLOSURE

An input digital signal is periodically and alternately subjected to first modulation and second modulation, being thereby converted into a pair of a baseband I signal and a baseband Q signal. The first modulation and the second modulation are different from each other. The pair of the baseband I signal and the baseband Q signal are outputted. The first modulation may be at least 8-signal-point modulation while the second modulation may be phase shift keying.

Document Page 114 of 119

66T020" 2E90+260

FIG. 1

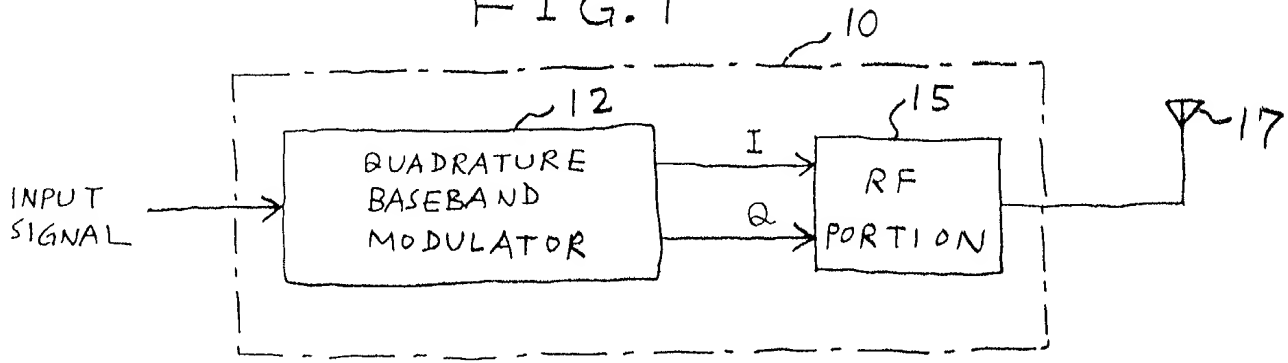


FIG. 3

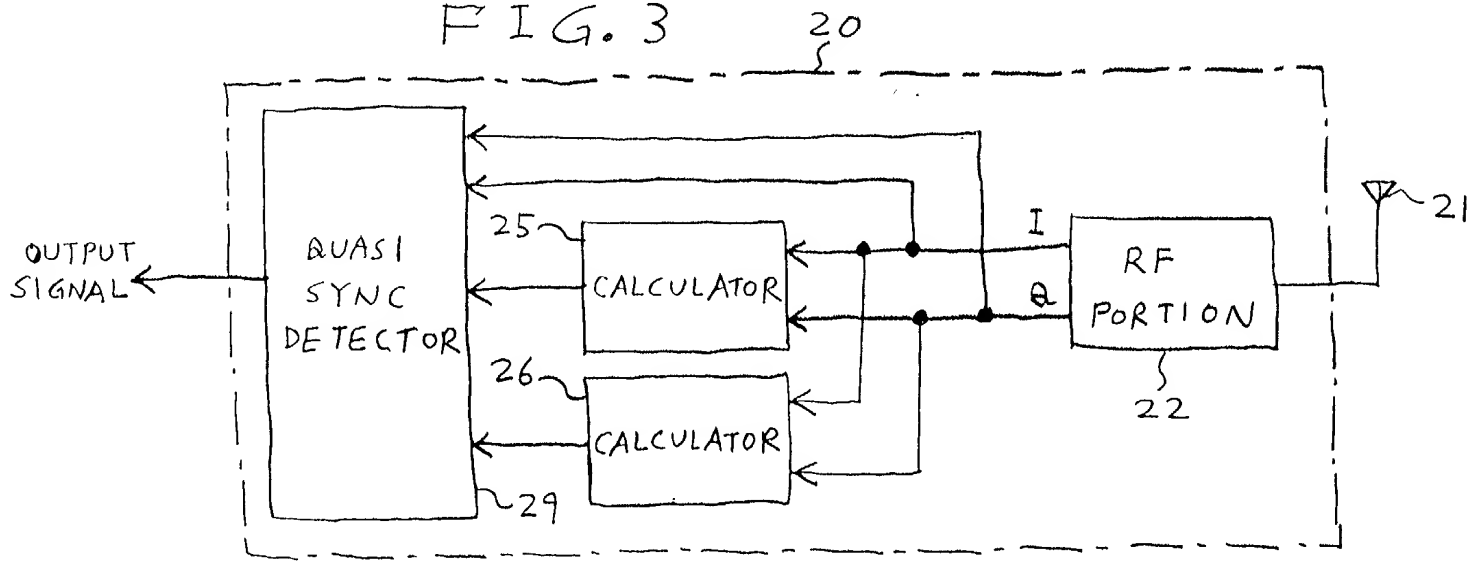


FIG. 2

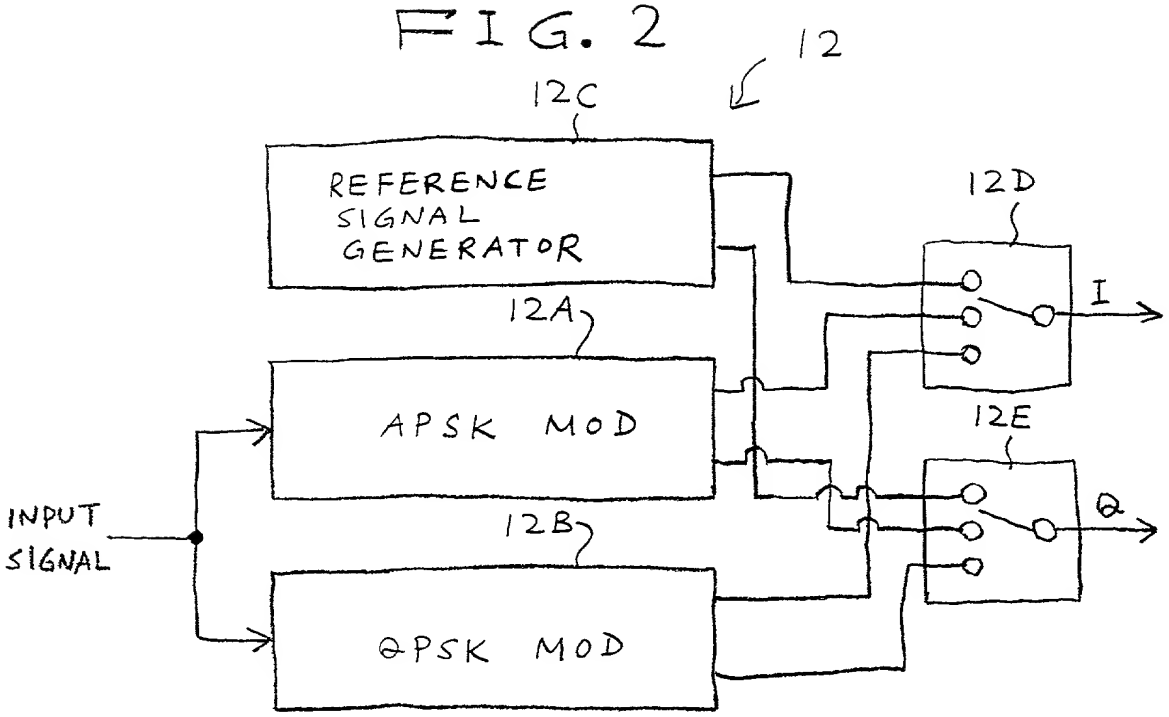

12
12C
REFERENCE SIGNAL GENERATOR
12D
I
12A
APSK MOD
12E
Q
INPUT SIGNAL
12B
QPSK MOD

FIG. 4

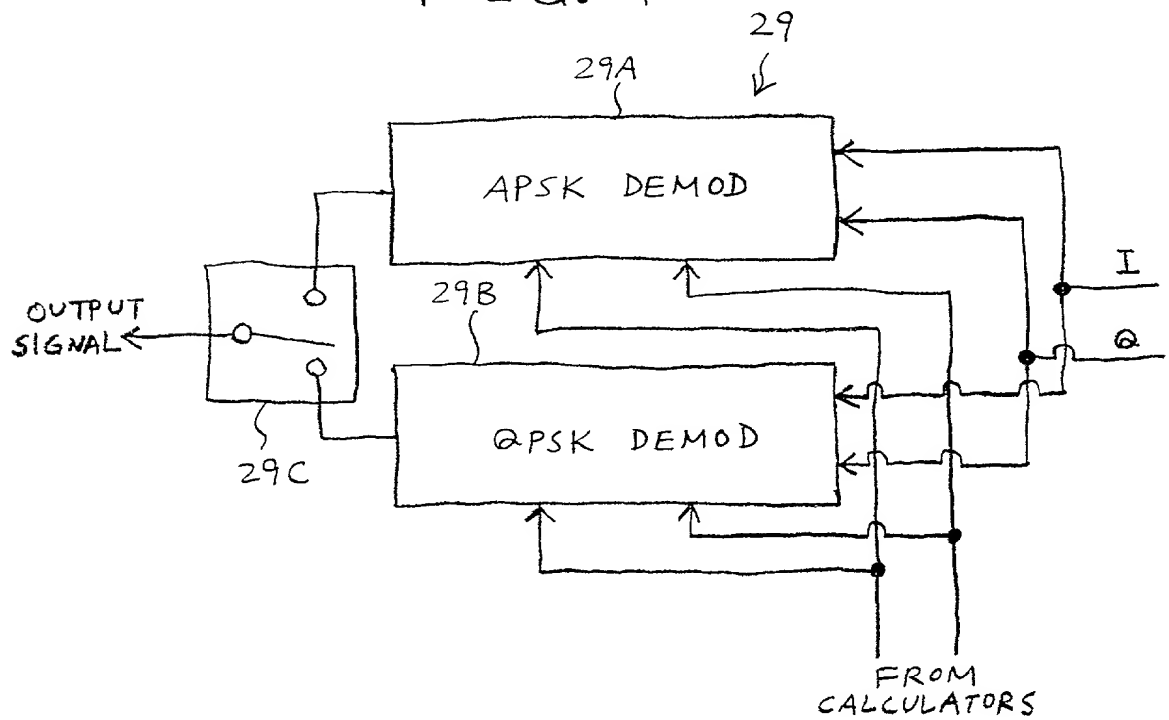

29
29A
APSK DEMOD
I
Q
OUTPUT SIGNAL
29B
QPSK DEMOD
29C
FROM CALCULATORS

FIG. 5

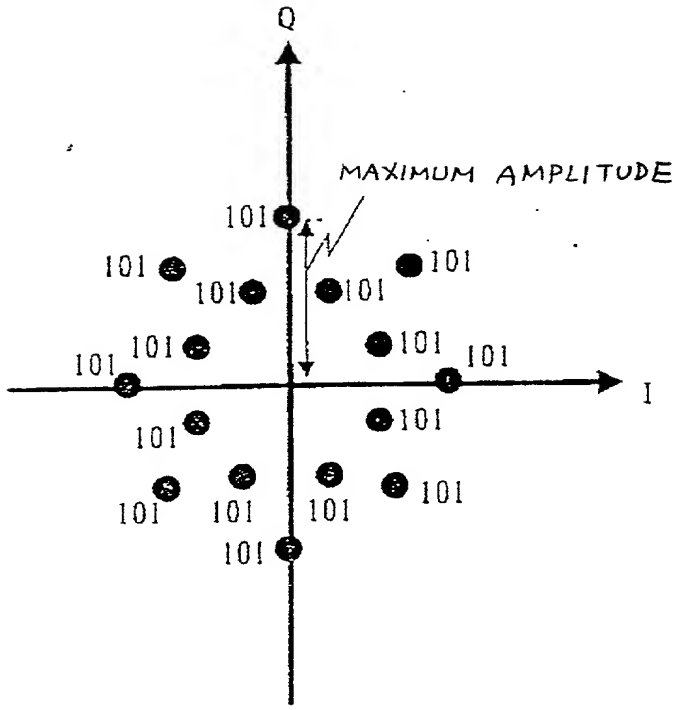
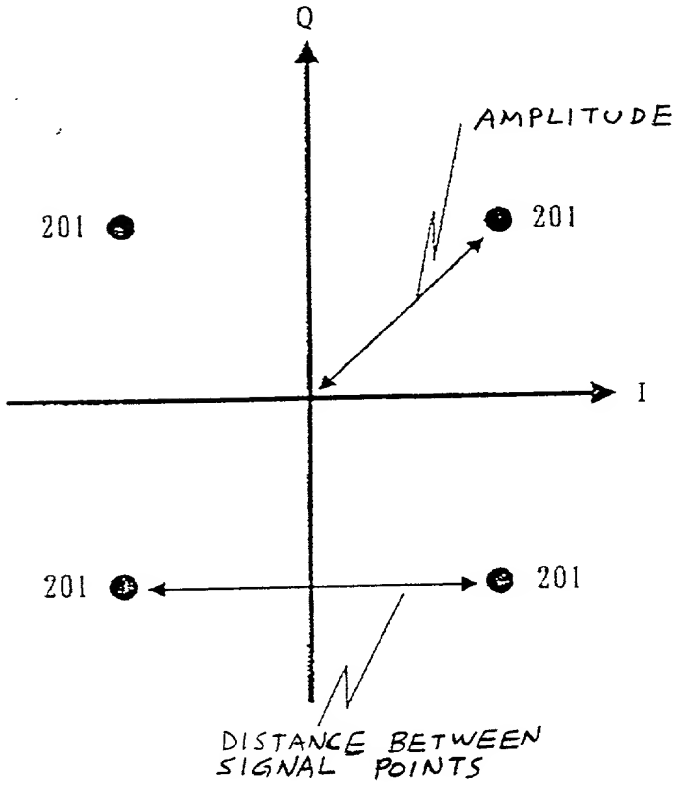


FIG. 6



EP 0 752 768 B1

FIG. 7

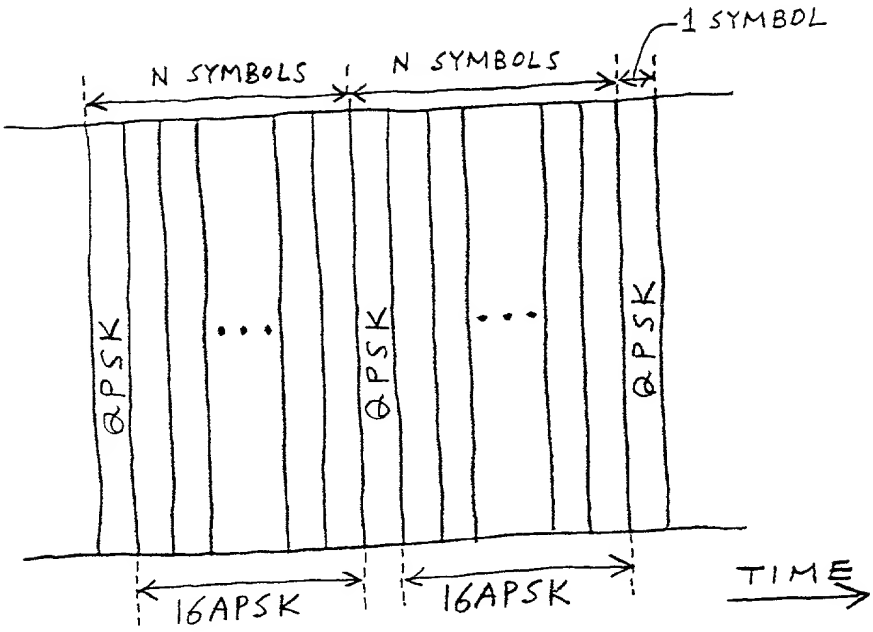

1 SYMBOL
N SYMBOLS
N SYMBOLS
QPSK
QPSK
QPSK
16APSK
16APSK
TIME

FIG. 10

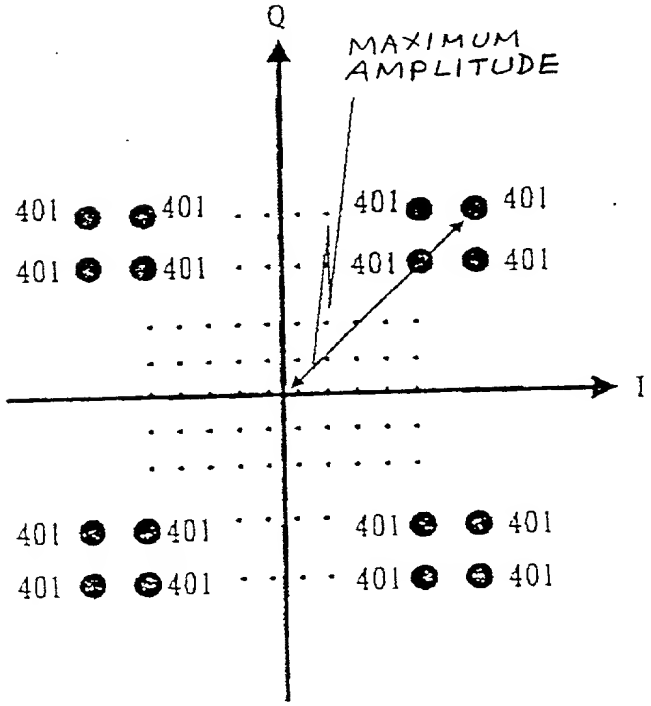

Q
MAXIMUM AMPLITUDE
I
401

FIG. 8

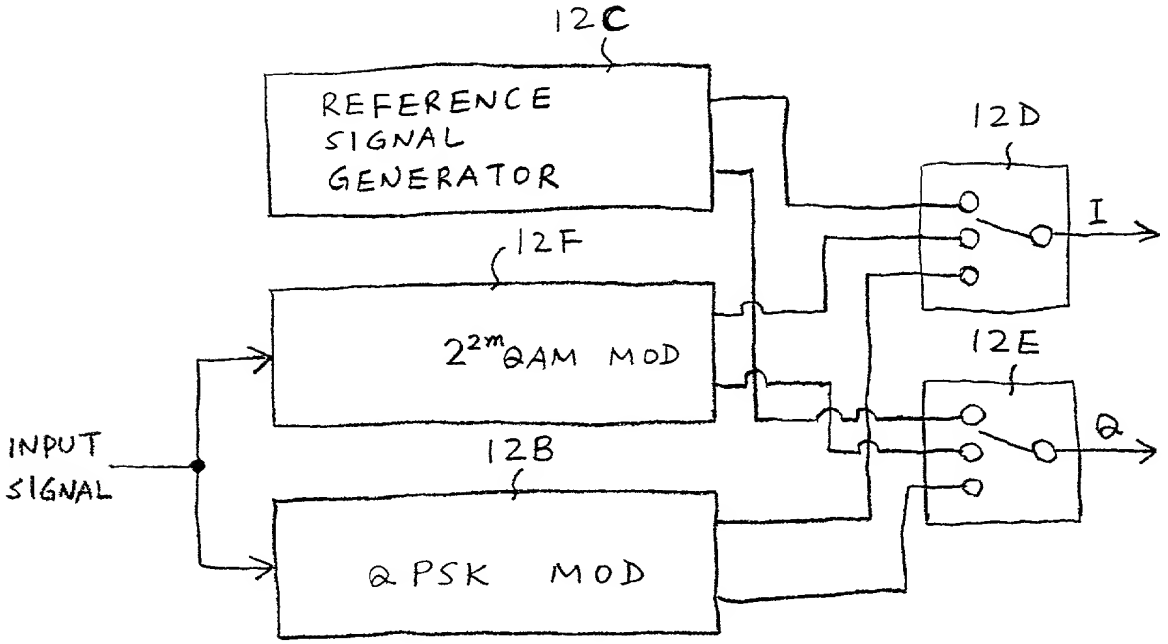

12C
REFERENCE SIGNAL GENERATOR
12D
I
12F
2^{2m}QAM MOD
12E
Q
INPUT SIGNAL
12B
QPSK MOD

FIG. 9

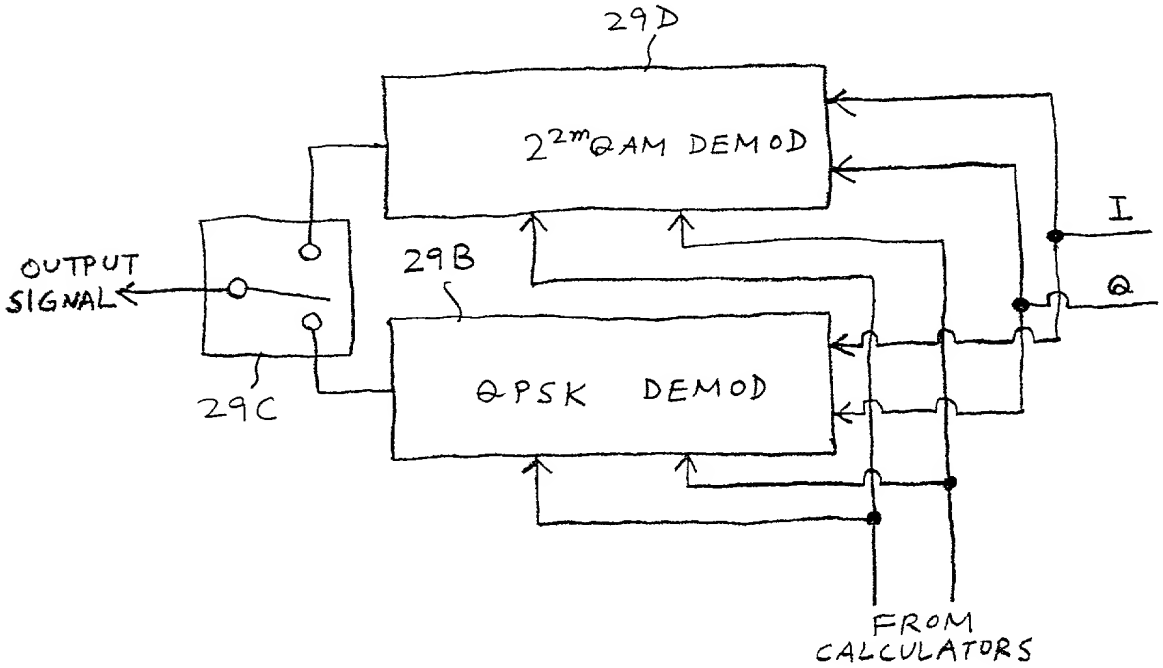

29D
2^{2m}QAM DEMOD
I
Q
OUTPUT SIGNAL
29B
29C
QPSK DEMOD
FROM CALCULATORS

FIG. 11

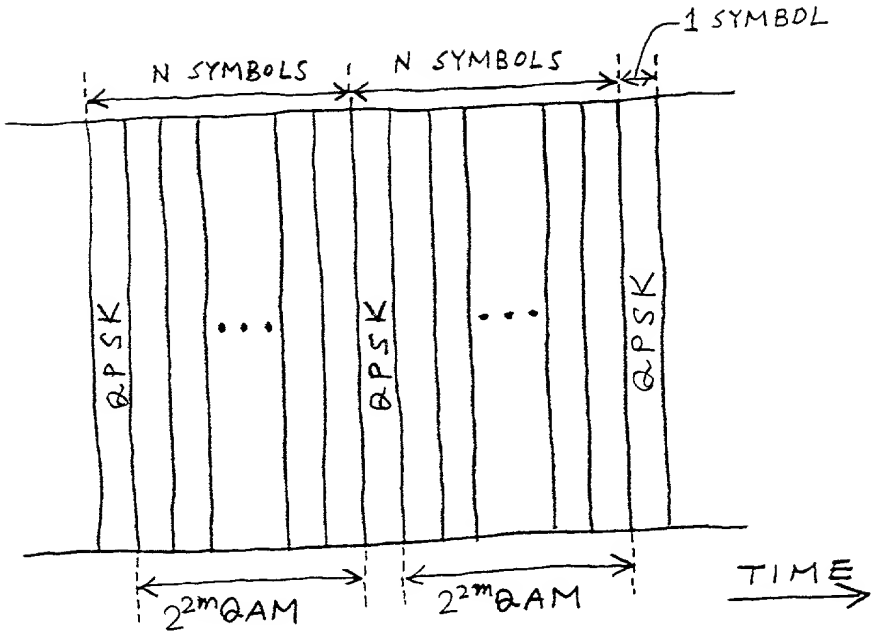

1 SYMBOL
N SYMBOLS
N SYMBOLS
QPSK
QPSK
QPSK
2^{2m}QAM
2^{2m}QAM
TIME

FIG. 12

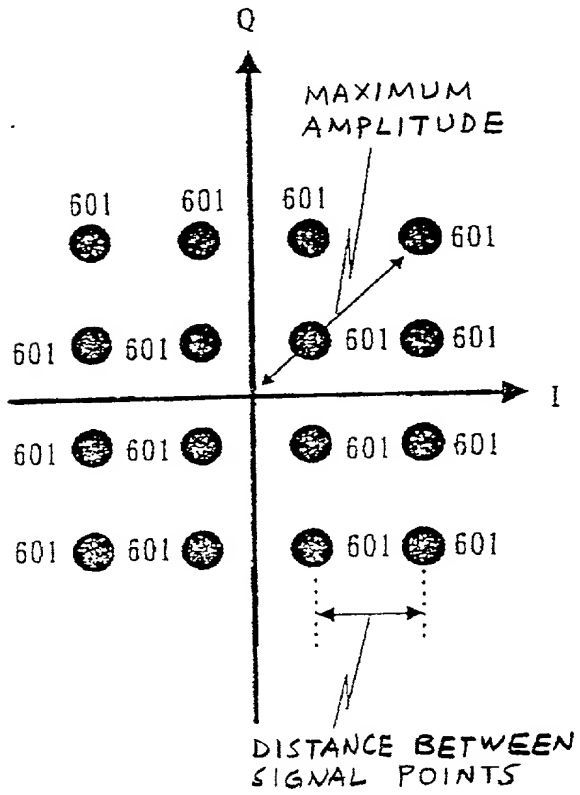

Q
I
MAXIMUM AMPLITUDE
601
DISTANCE BETWEEN SIGNAL POINTS

FIG. 13

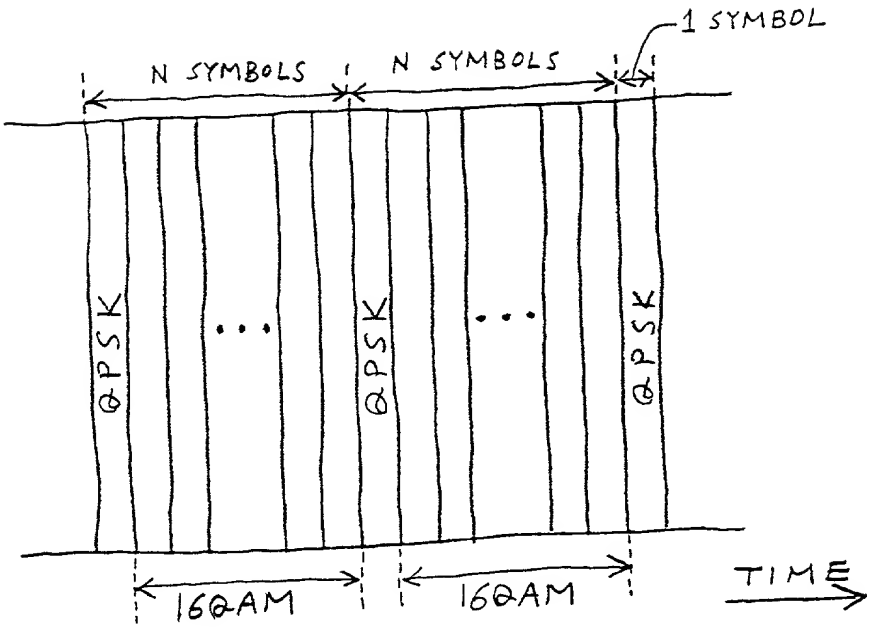

1 SYMBOL
N SYMBOLS
N SYMBOLS
QPSK
QPSK
QPSK
16QAM
16QAM
TIME

FIG. 15

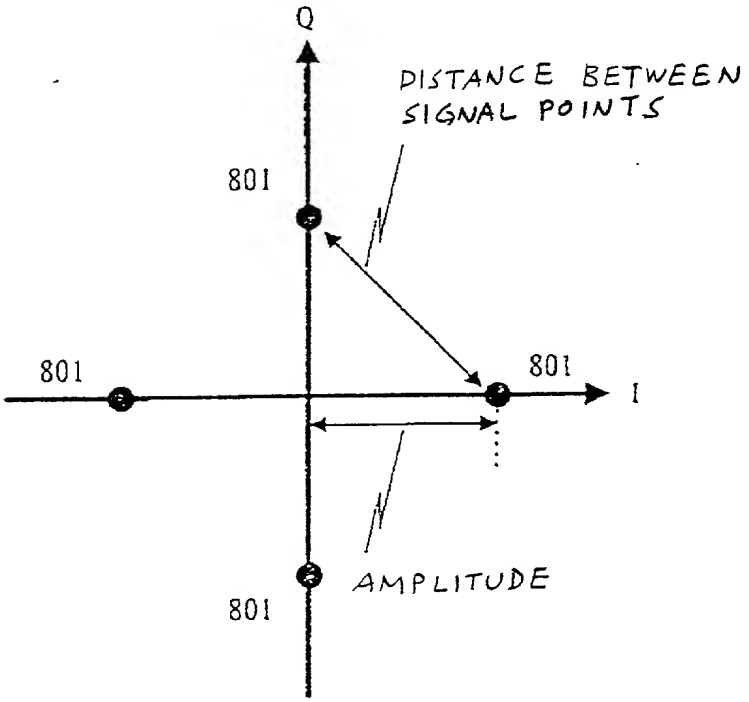

Q
DISTANCE BETWEEN SIGNAL POINTS
801
801
801
I
AMPLITUDE
801

FIG. 14

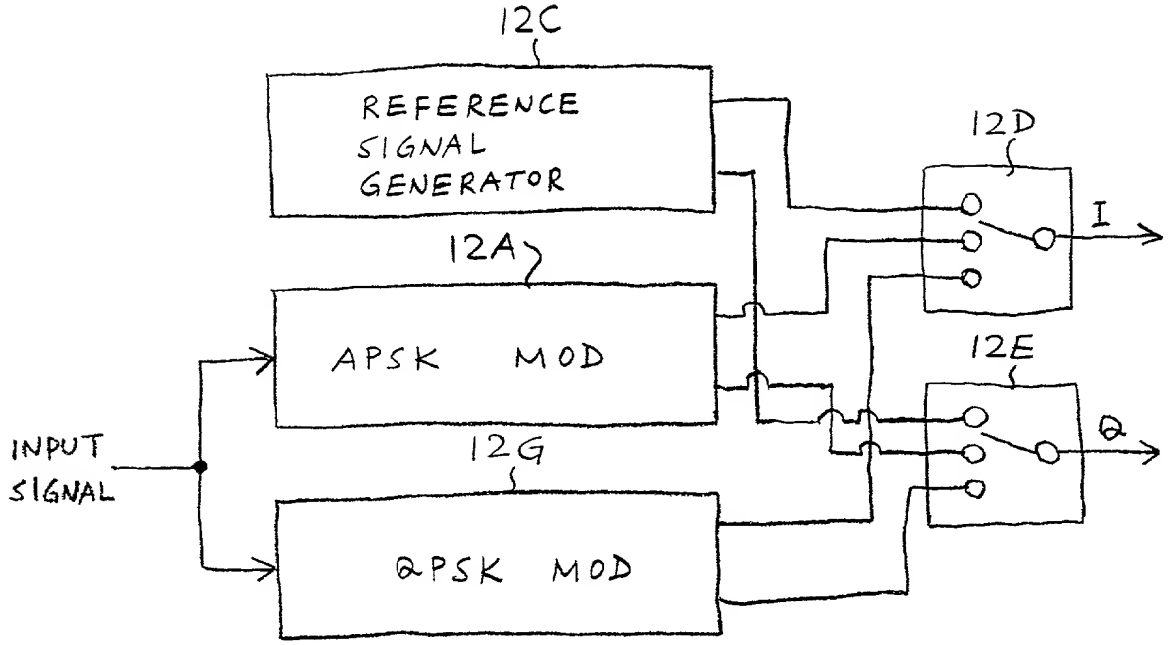

12C
REFERENCE SIGNAL GENERATOR
12D
I
12A
APSK MOD
12E
Q
INPUT SIGNAL
12G
QPSK MOD

FIG. 16

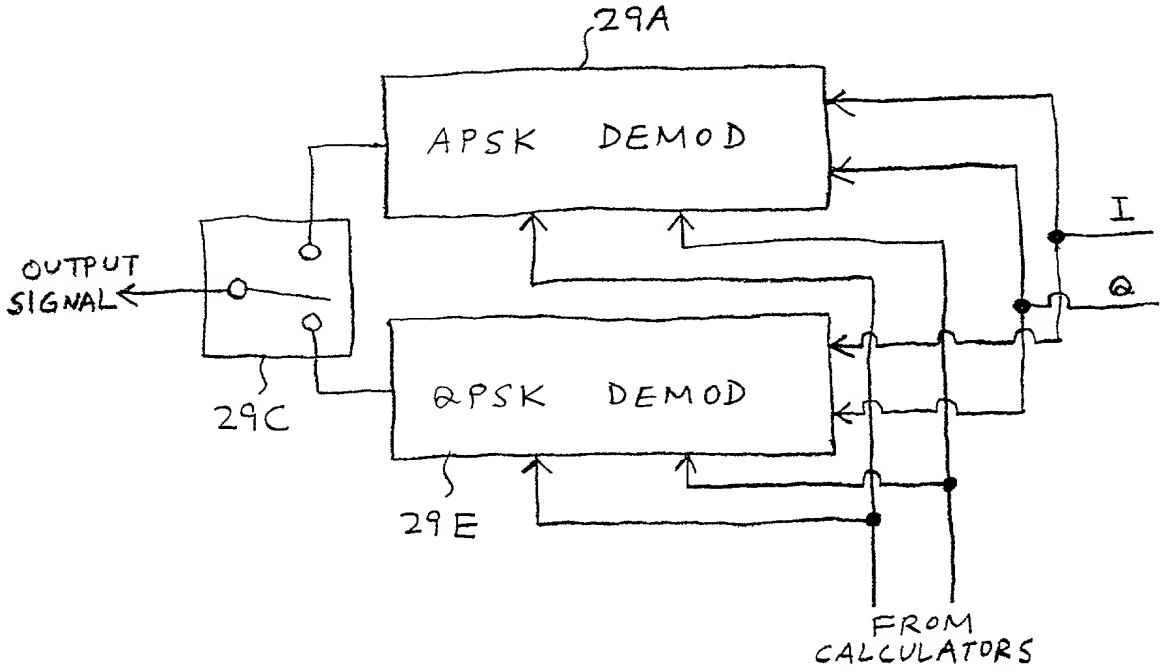

29A
APSK DEMOD
I
Q
OUTPUT SIGNAL
29C
QPSK DEMOD
29E
FROM CALCULATORS

FIG. 17

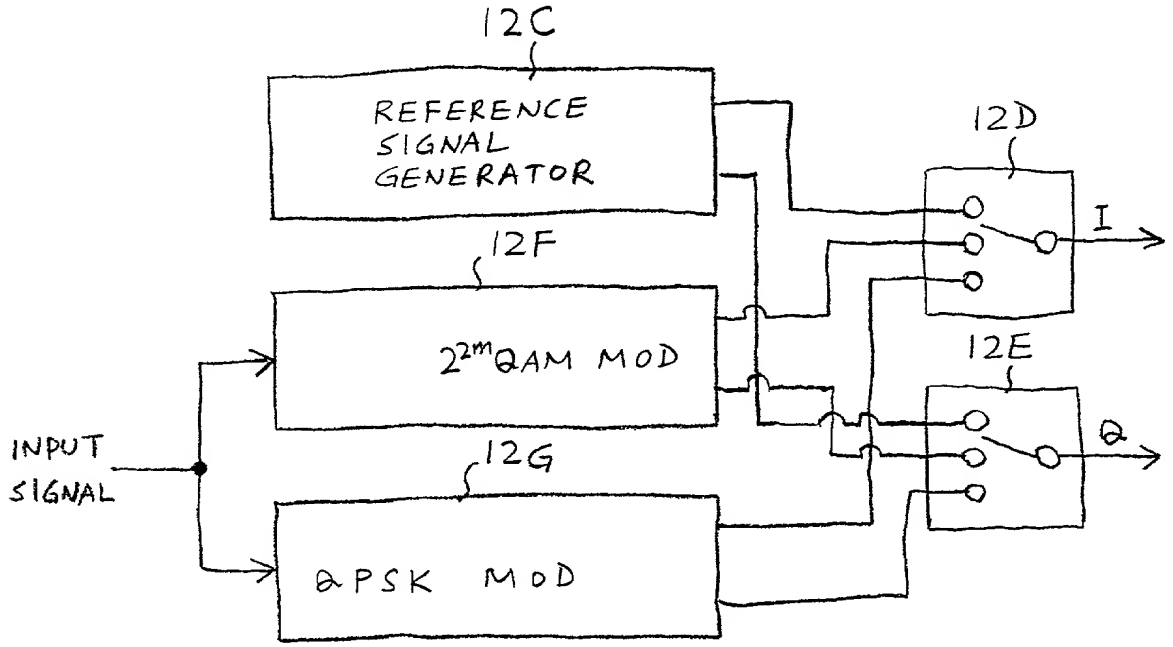
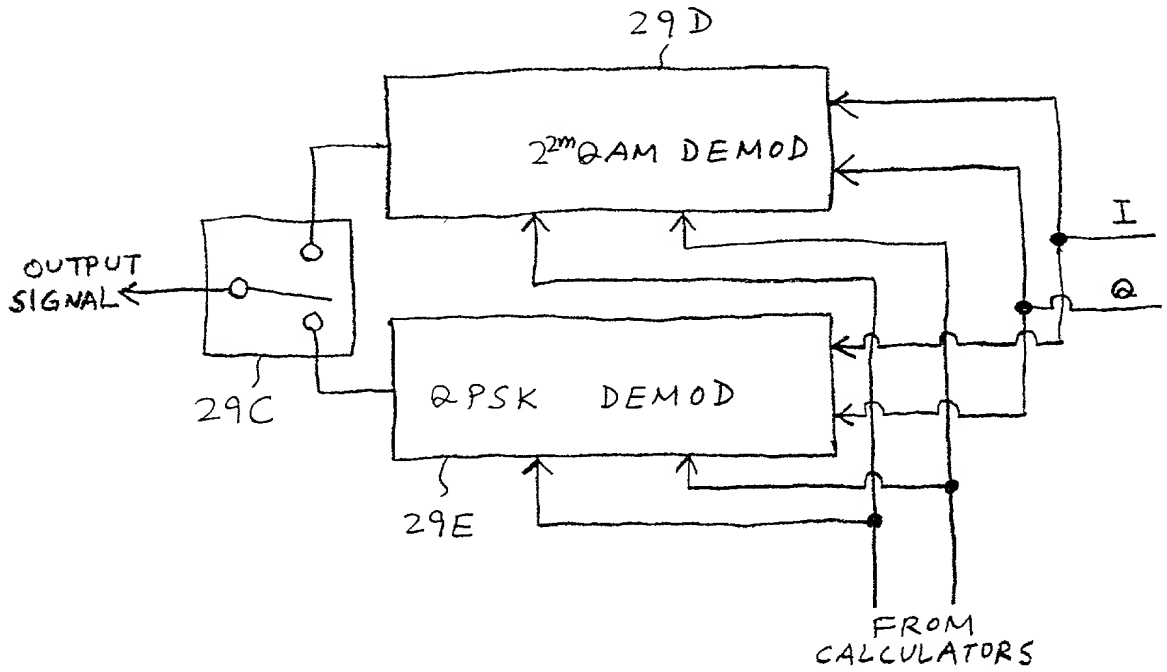


FIG. 18



Petitioner - Apple Inc. EX1009 Page 16

FIG. 19

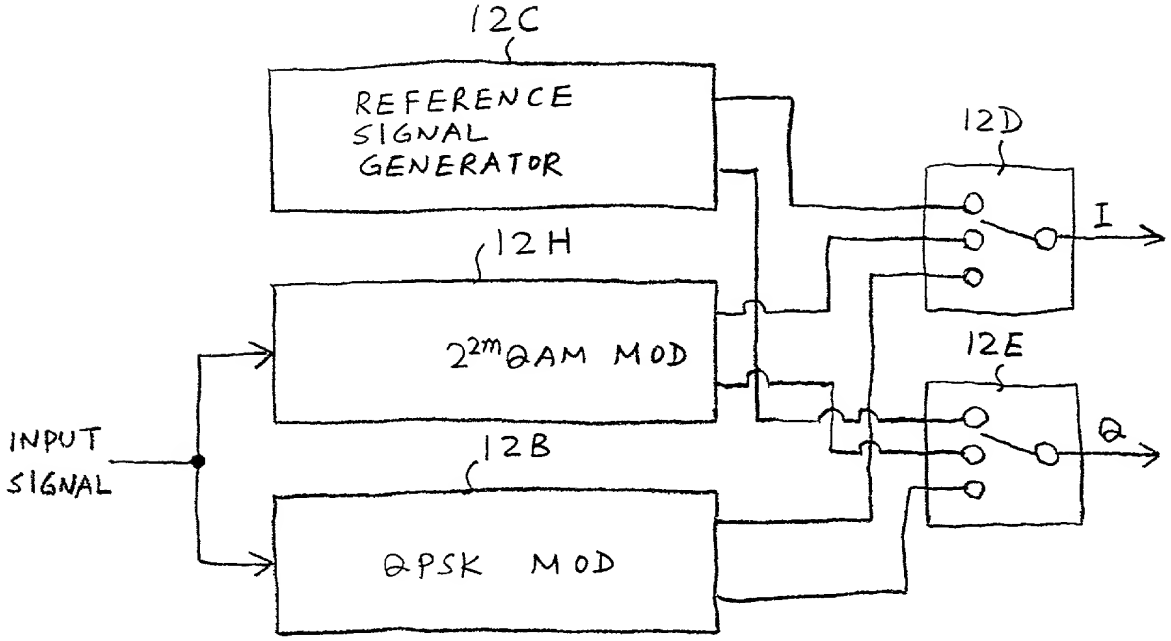
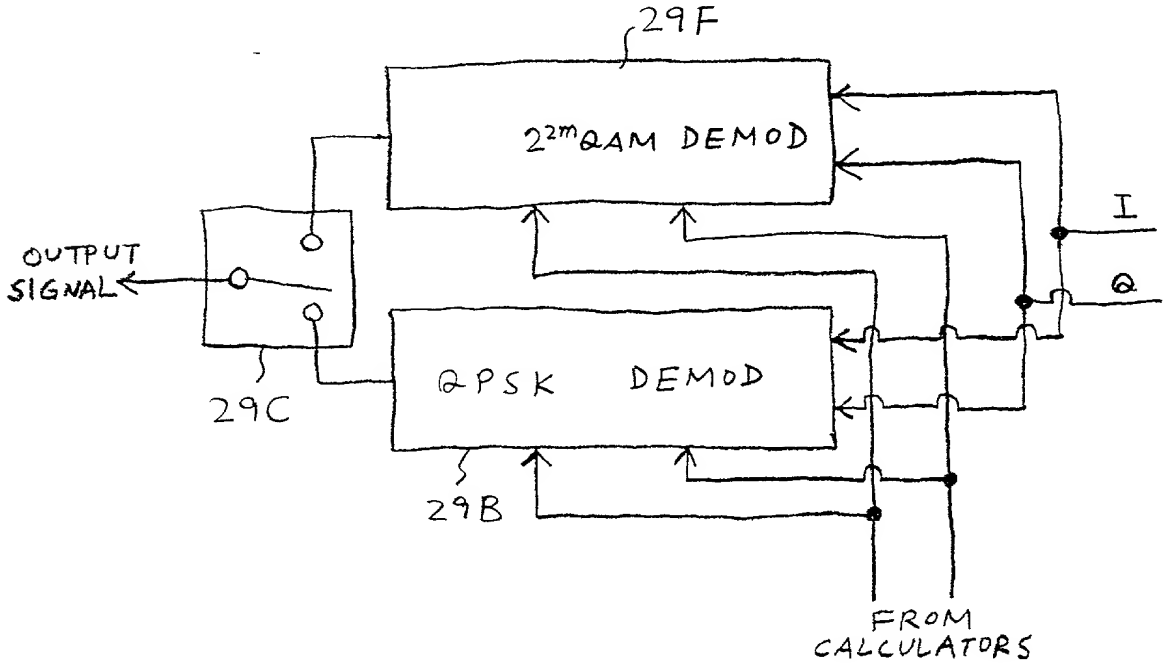


FIG. 20



Petitioner's Exhibit 1009
Page 23 of 29

FIG. 21

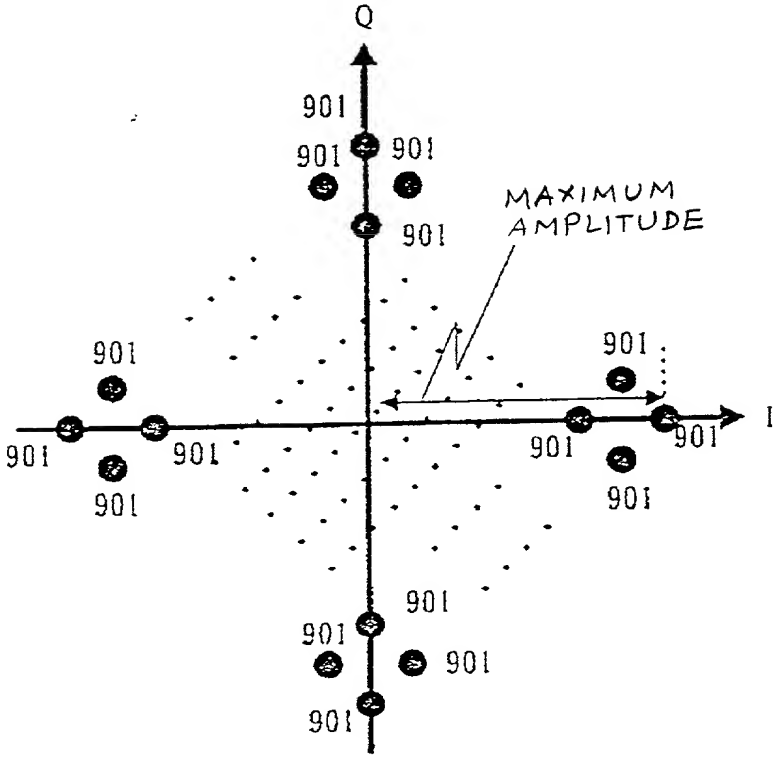

Q
I
MAXIMUM AMPLITUDE
901

FIG. 22

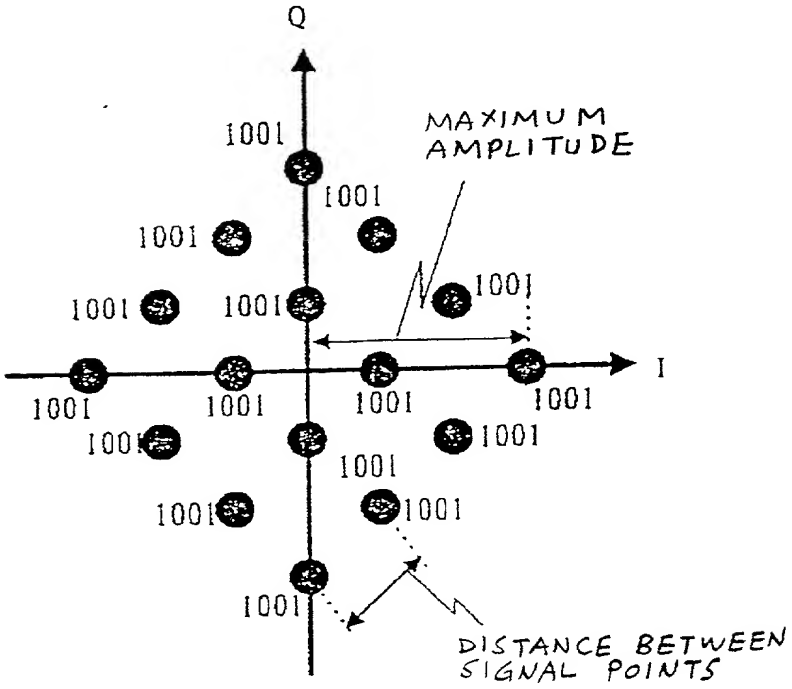

Q
I
MAXIMUM AMPLITUDE
1001
DISTANCE BETWEEN SIGNAL POINTS

FIG. 23

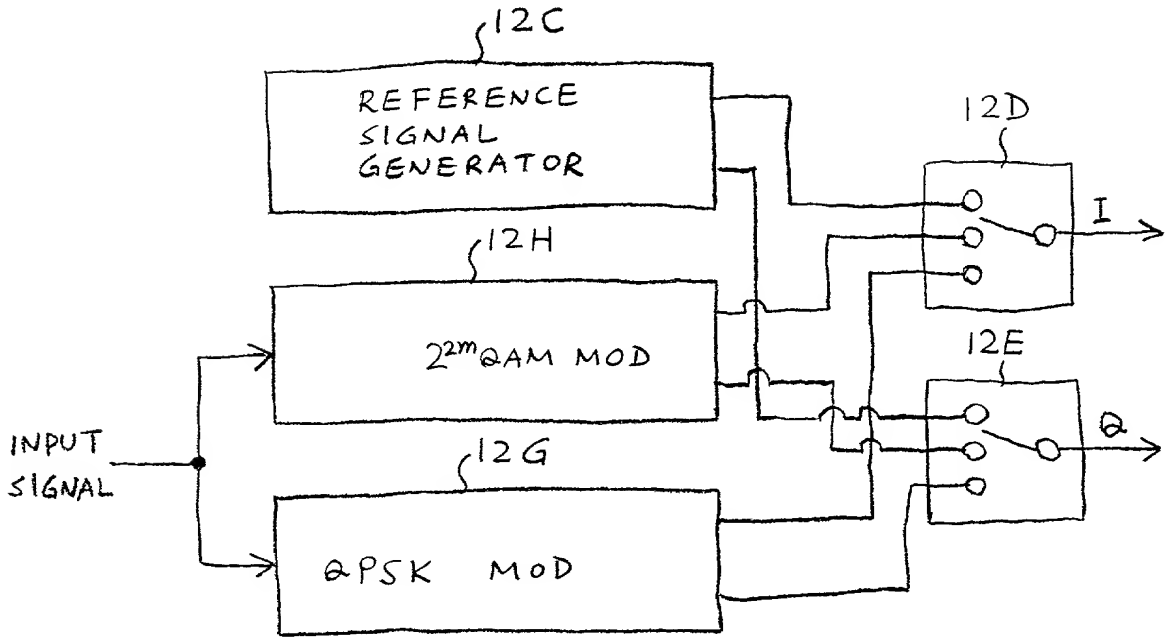

12C
REFERENCE SIGNAL GENERATOR
12D
I
12H
2^{2m}QAM MOD
12E
Q
INPUT SIGNAL
12G
QPSK MOD

FIG. 24

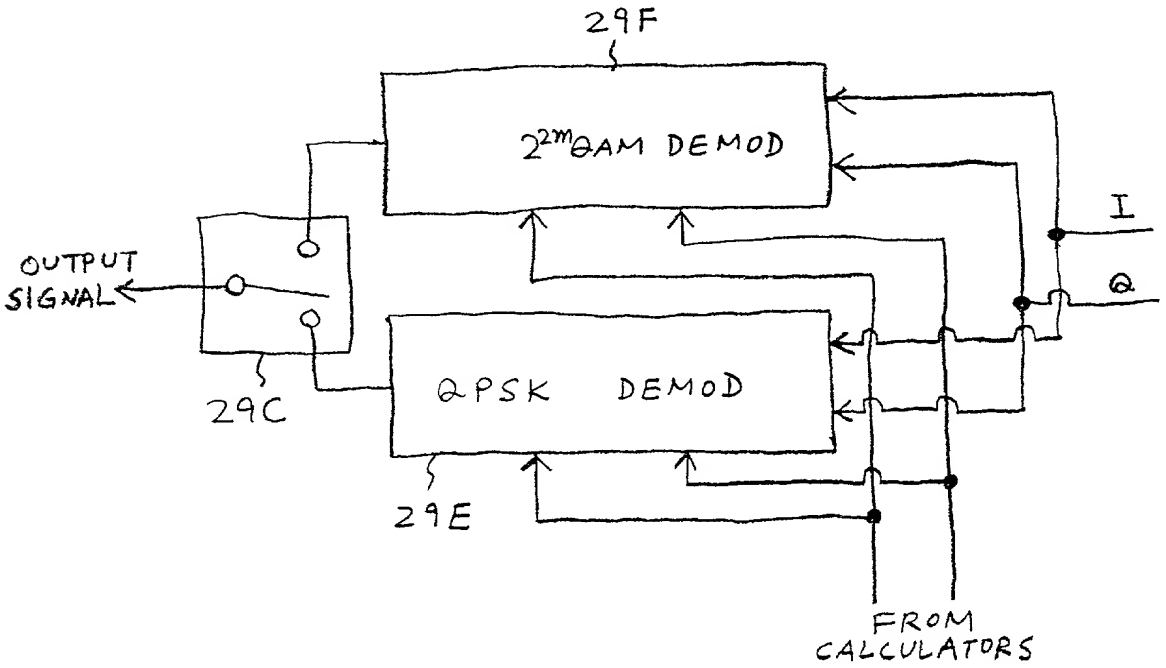

29F
2^{2m}QAM DEMOD
I
Q
OUTPUT SIGNAL
29C
QPSK DEMOD
29E
FROM CALCULATORS

FIG. 25

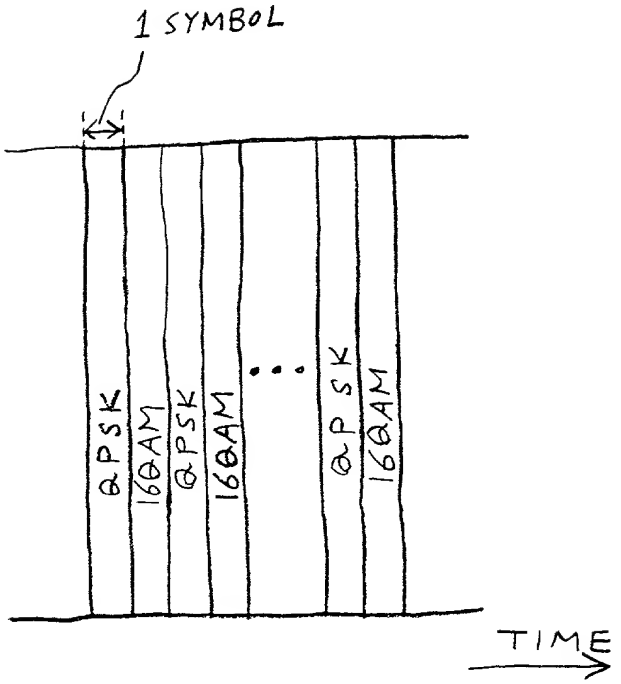


FIG. 26

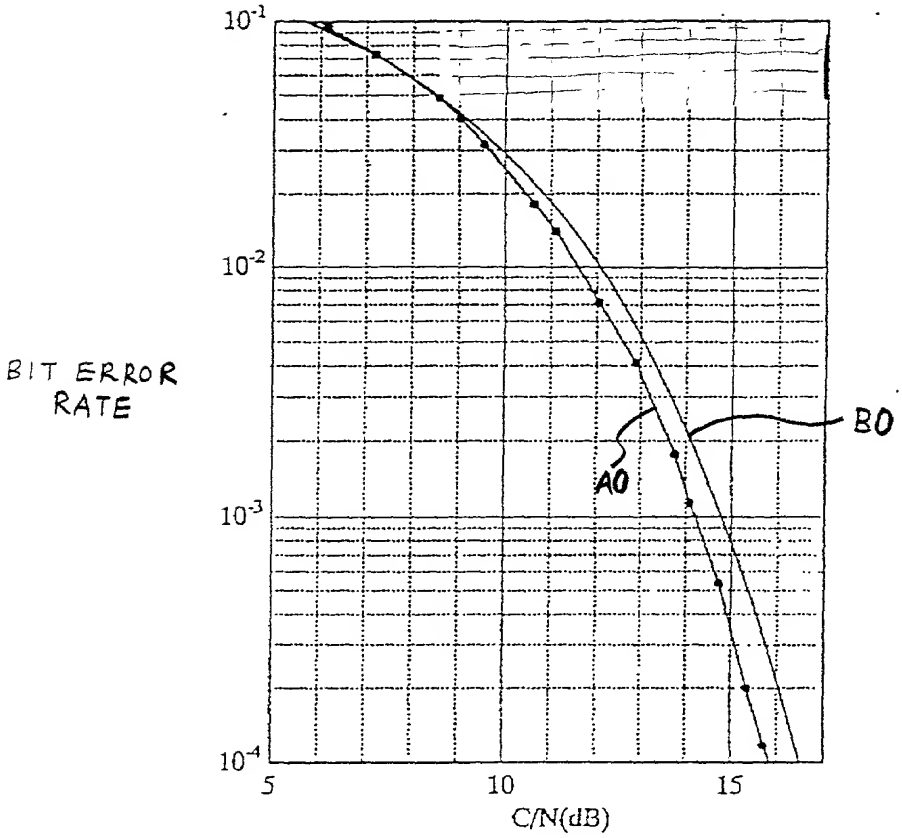


FIG. 27

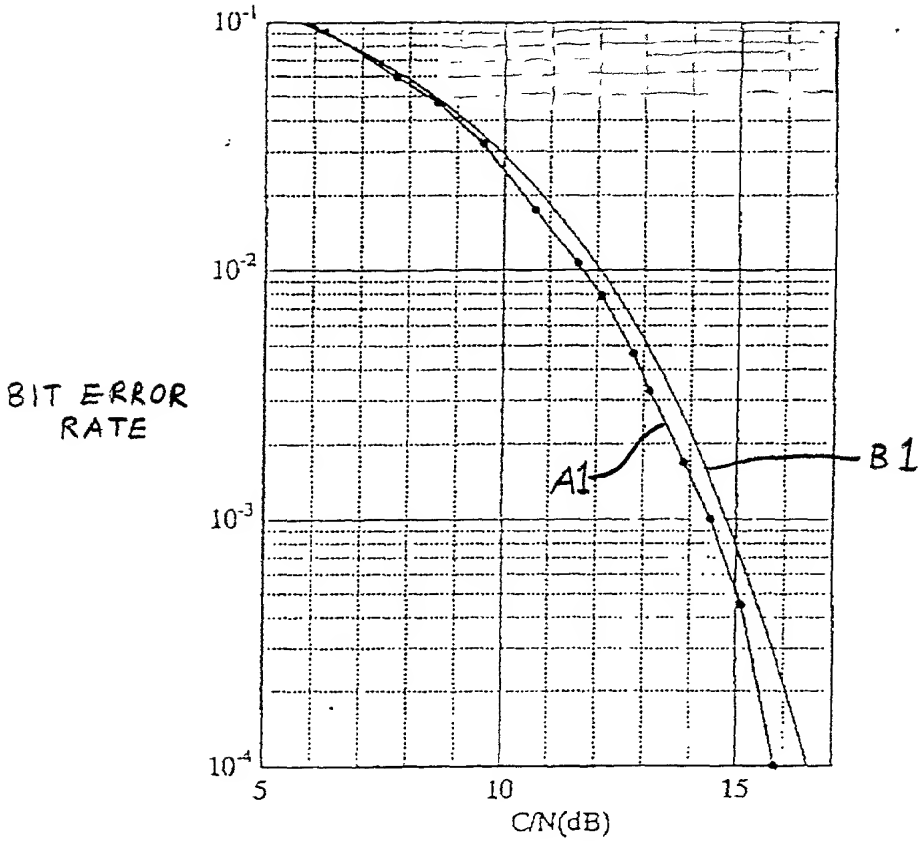


FIG. 28

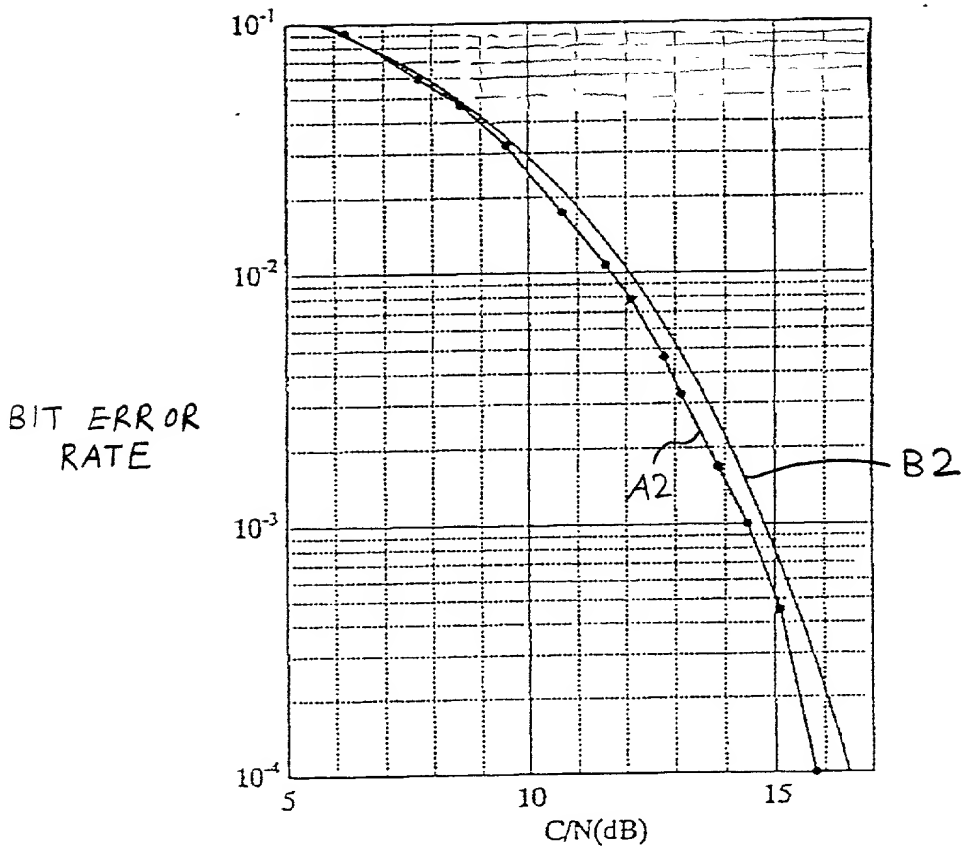
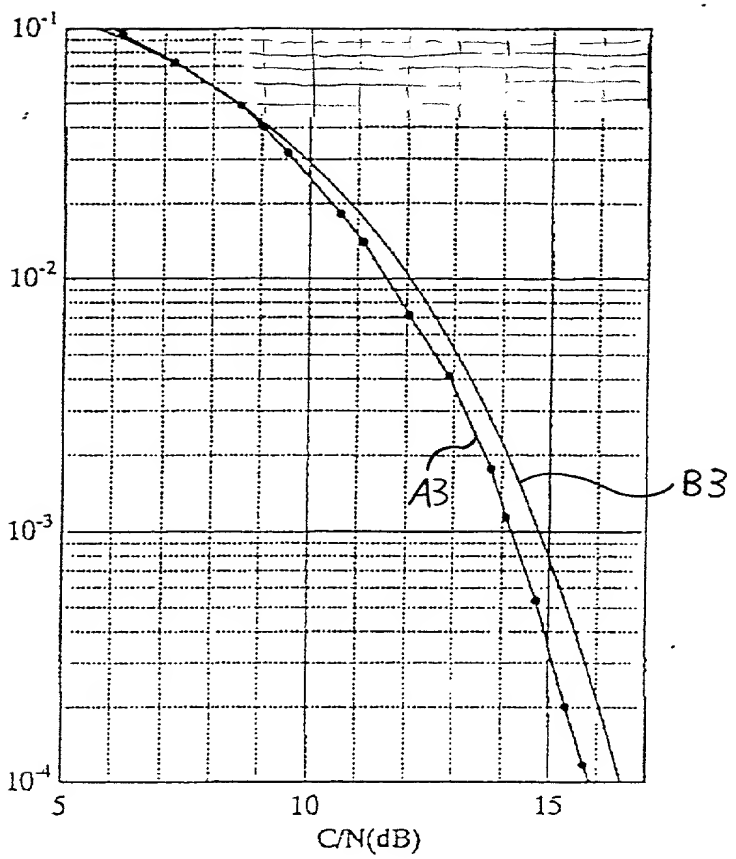


FIG. 29



661020 "2E90+260

FIG. 30

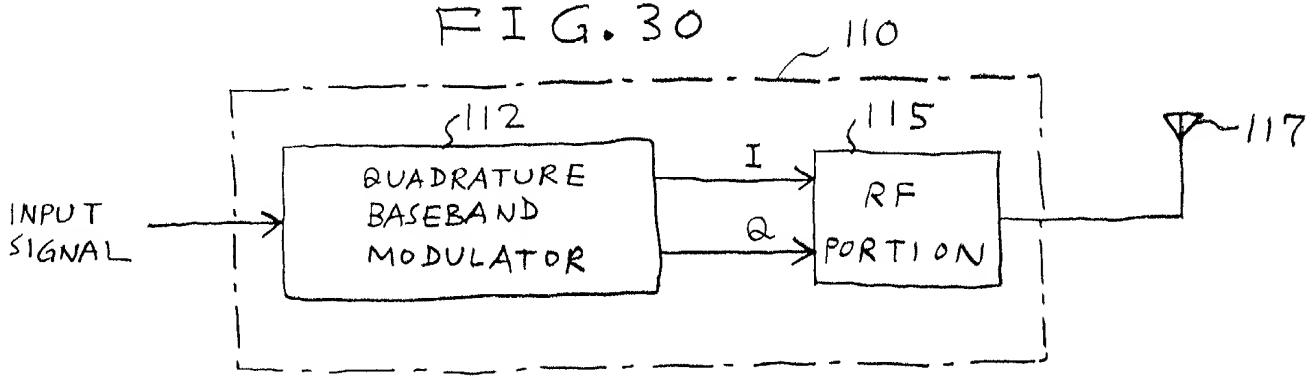


FIG. 32

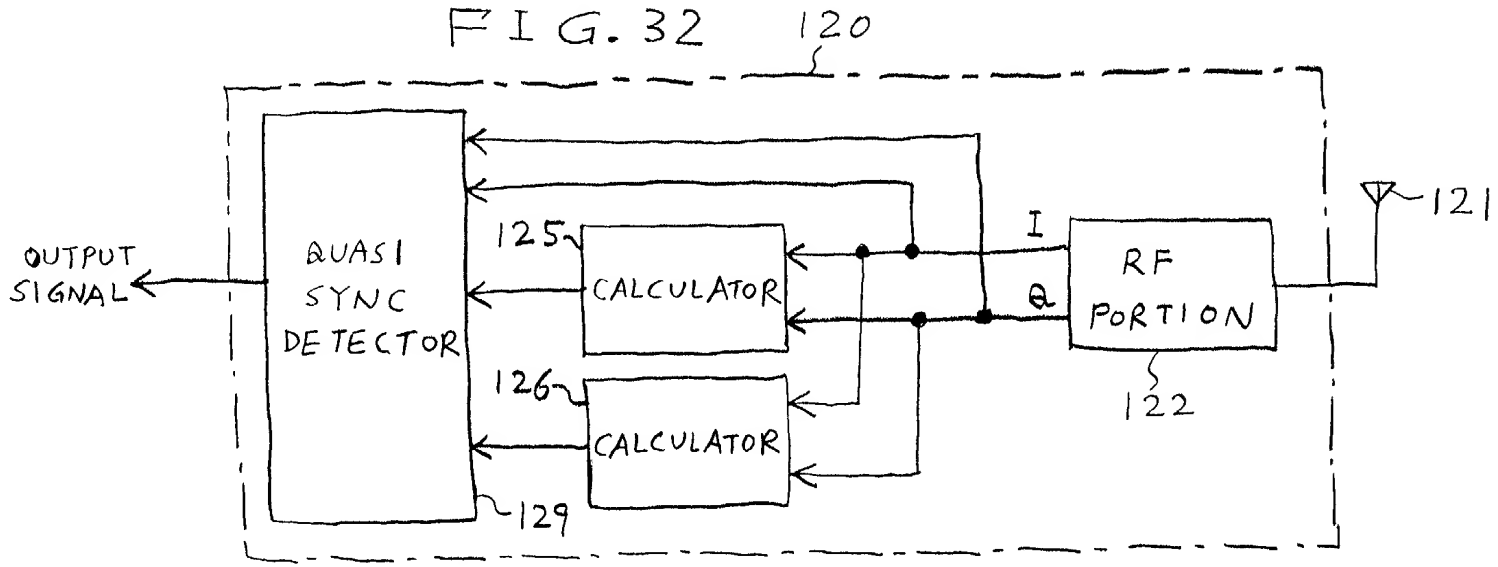


FIG. 31

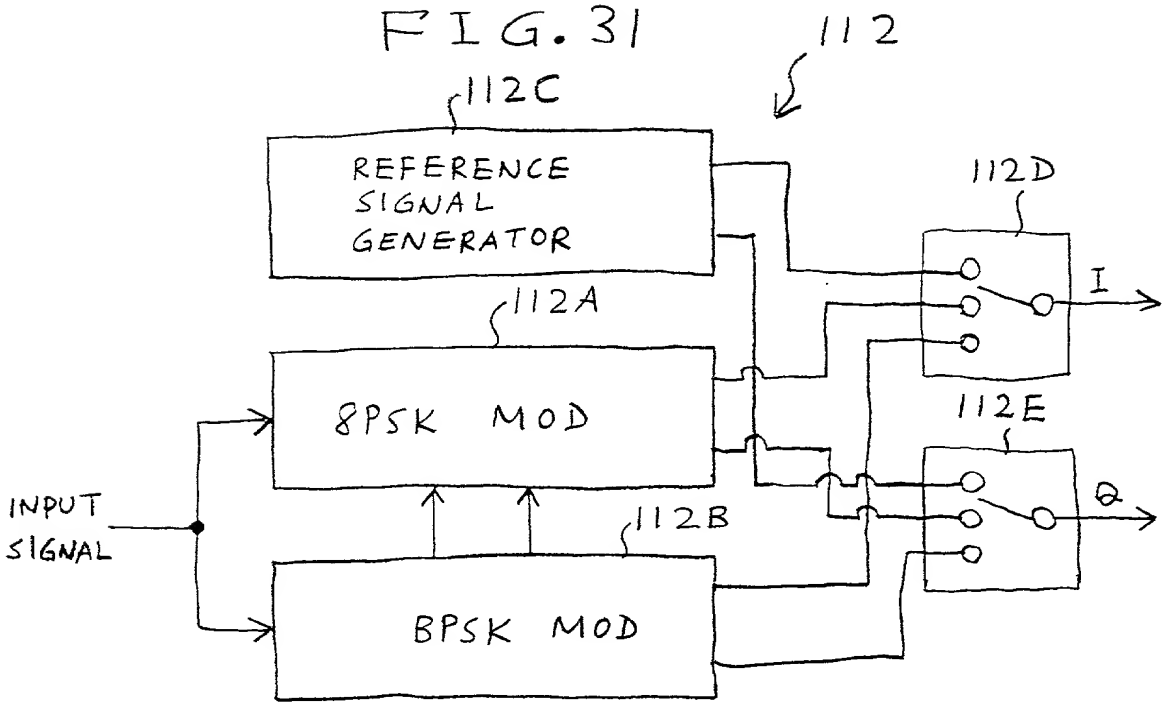

112
112C
REFERENCE SIGNAL GENERATOR
112D
I
112A
8PSK MOD
112E
Q
INPUT SIGNAL
112B
BPSK MOD

FIG. 33

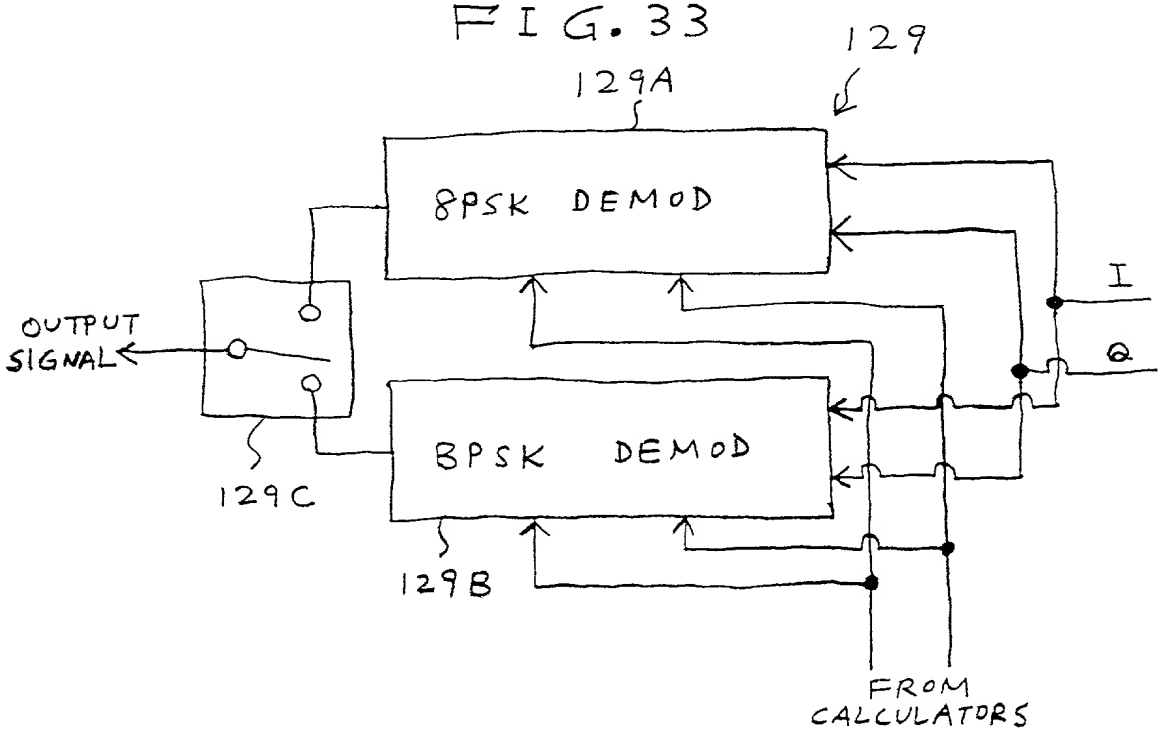

129
129A
8PSK DEMOD
I
Q
OUTPUT SIGNAL
BPSK DEMOD
129C
129B
FROM CALCULATORS

FIG. 34

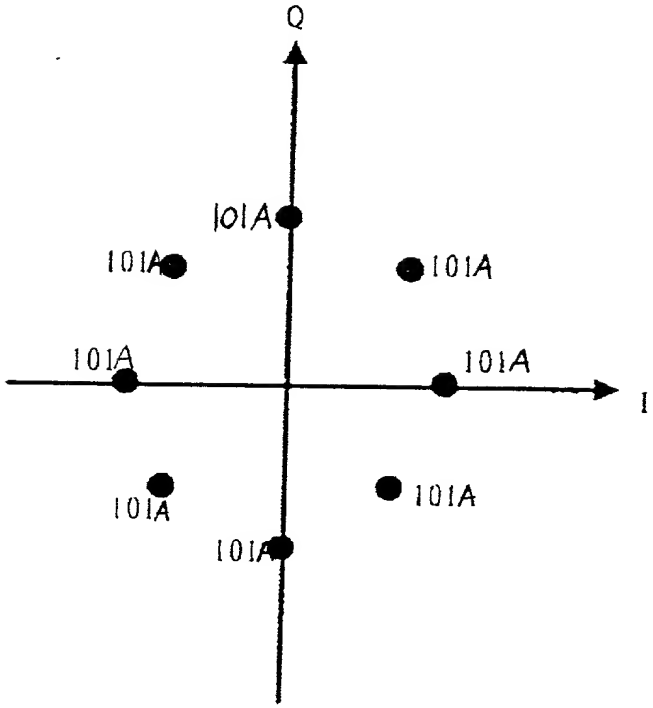


FIG. 35

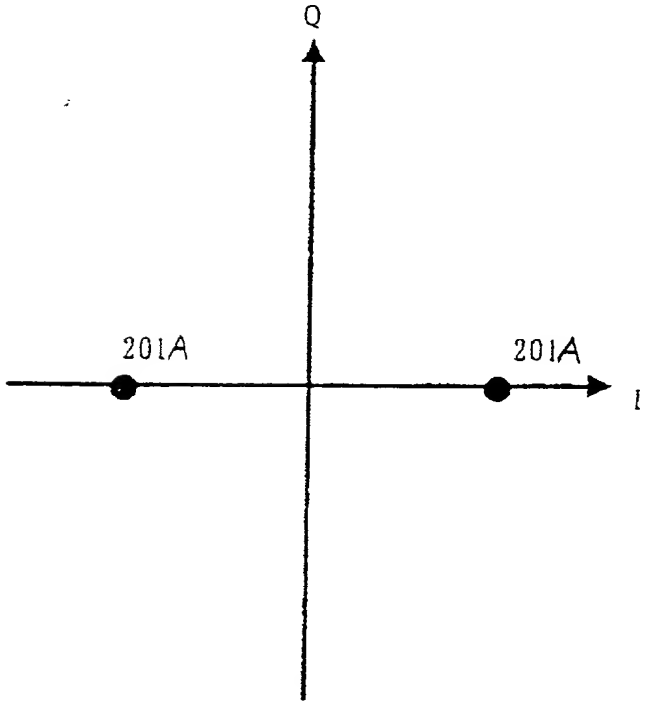


FIG. 36

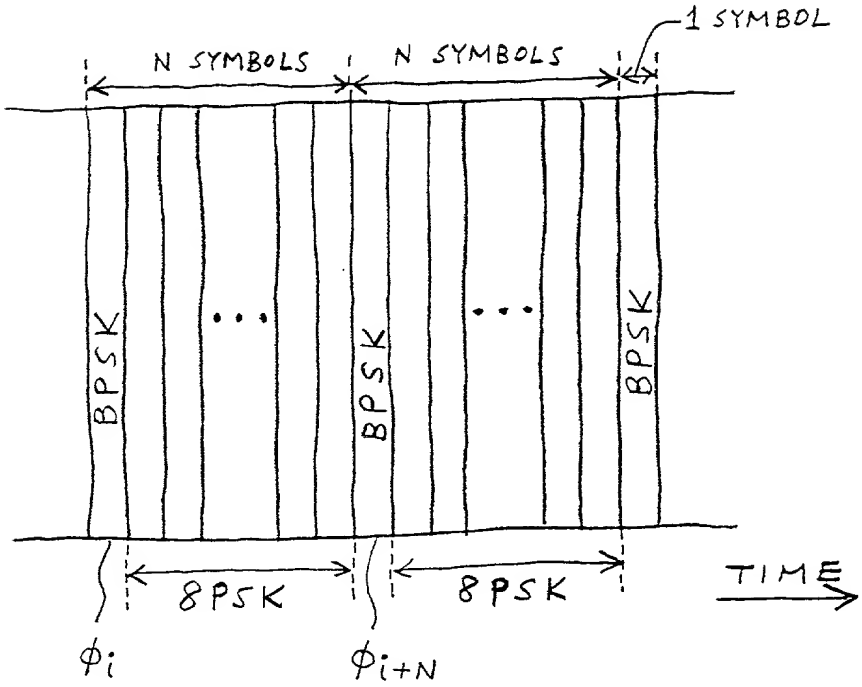

1 SYMBOL
N SYMBOLS
N SYMBOLS
BPSK
BPSK
BPSK
8PSK
8PSK
TIME
ϕ_i
ϕ_{i+N}

FIG. 37

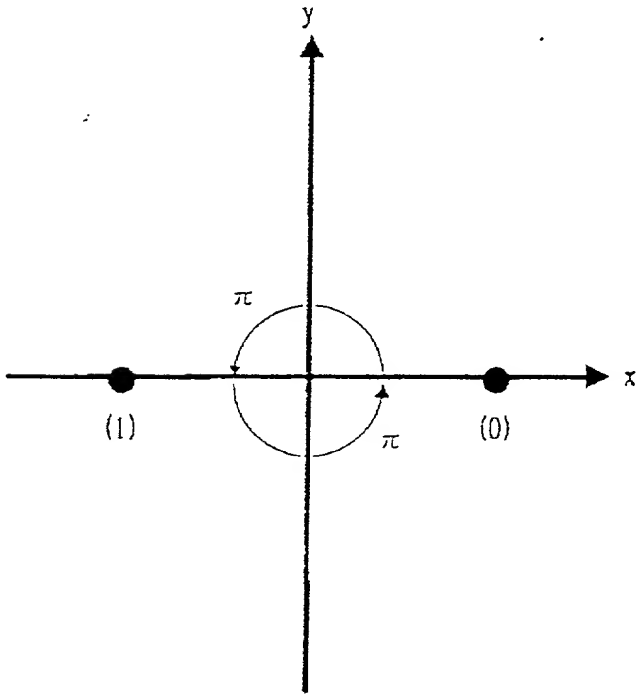

y
x
π
π
(1)
(0)

FIG. 38

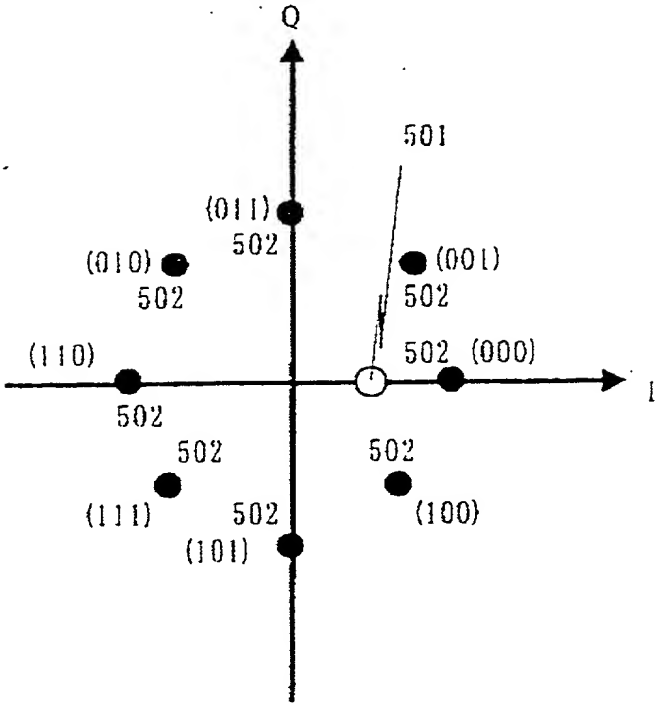

Q
I
501
(011)
502
(010)
502
(001)
502
(110)
502
502
(000)
502
502
(111)
502
(100)
502
(101)

FIG. 39

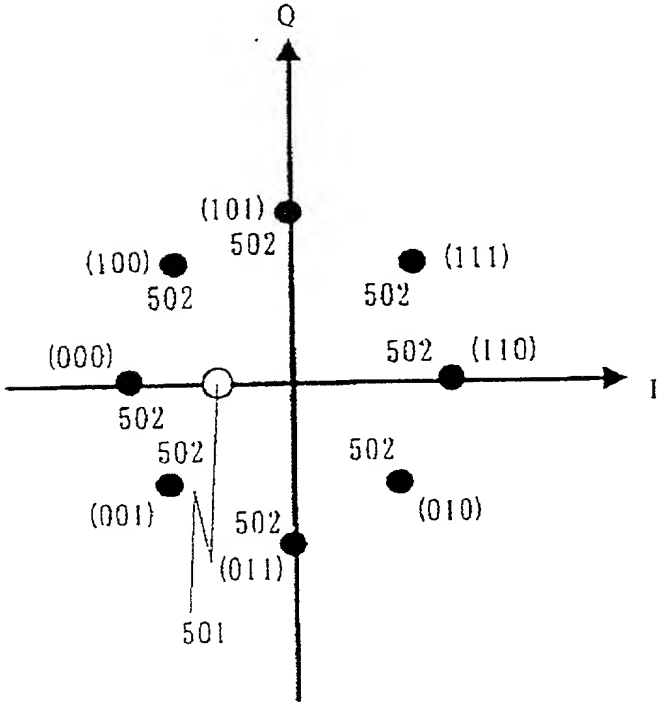

Q
I
(101)
502
(100)
502
(111)
502
(000)
502
502
(110)
502
502
(001)
502
(010)
502
(011)
501

FIG. 40

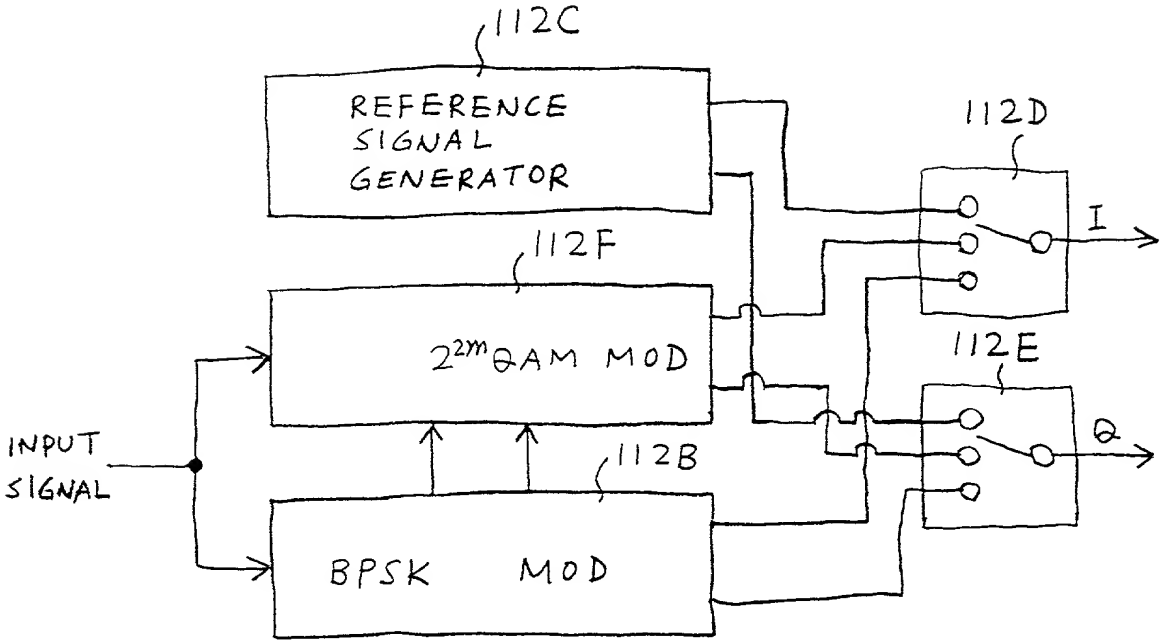

112C
REFERENCE SIGNAL GENERATOR
112D
I
112F
2^{2m}QAM MOD
112E
Q
INPUT SIGNAL
112B
BPSK MOD

FIG. 41

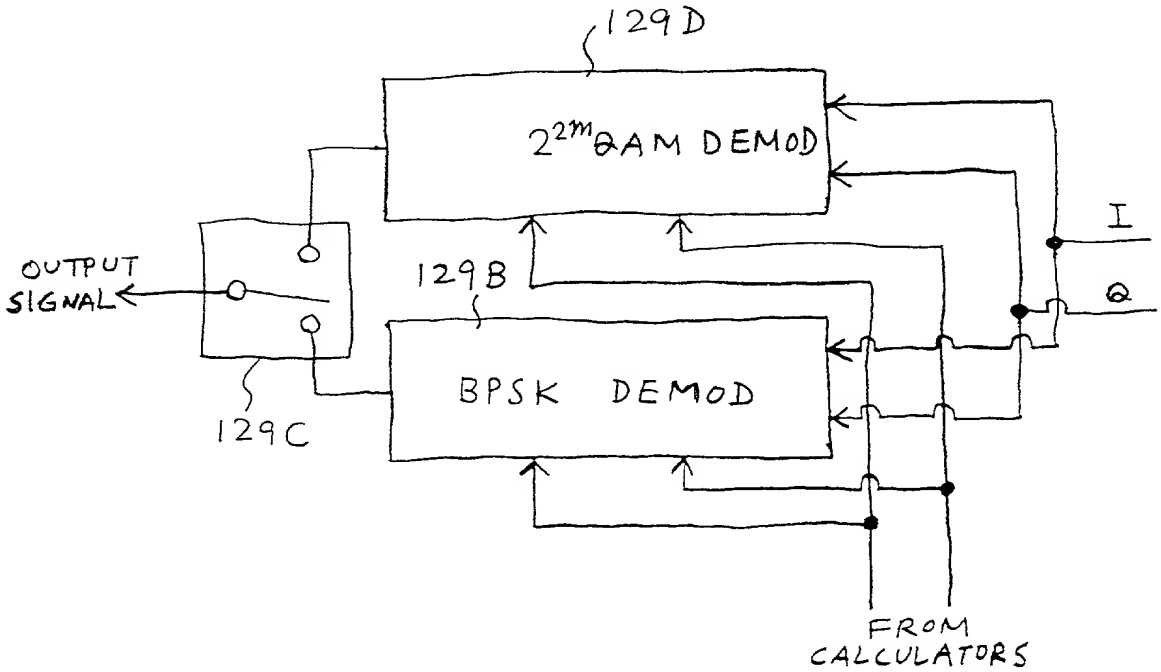

129D
2^{2m}QAM DEMOD
I
Q
OUTPUT SIGNAL
129B
BPSK DEMOD
129C
FROM CALCULATORS

FIG. 42

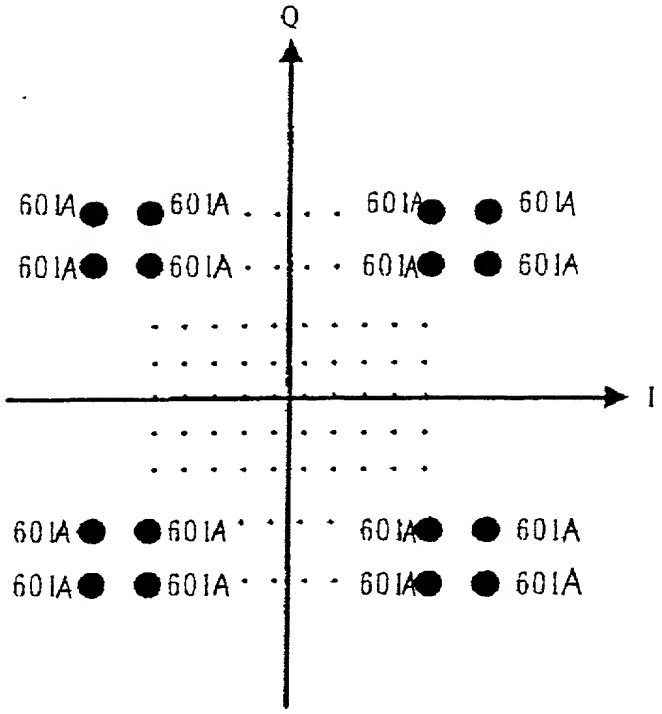


FIG. 43

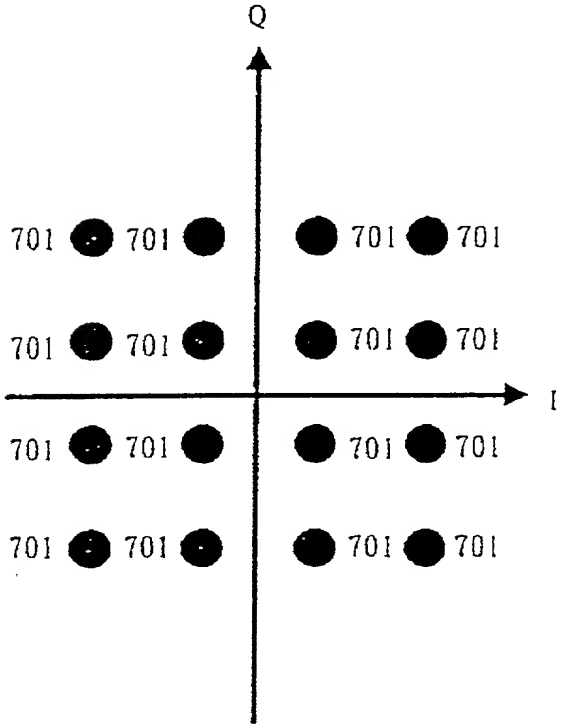


FIG. 44

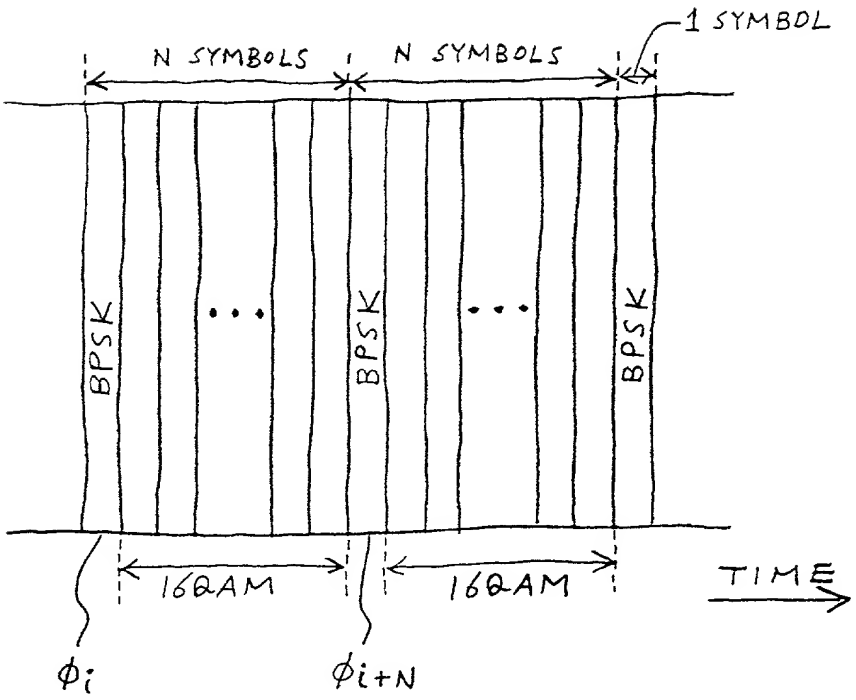

1 SYMBOL
N SYMBOLS
N SYMBOLS
BPSK
BPSK
BPSK
16QAM
16QAM
TIME
ϕ_i
ϕ_{i+N}

FIG. 45

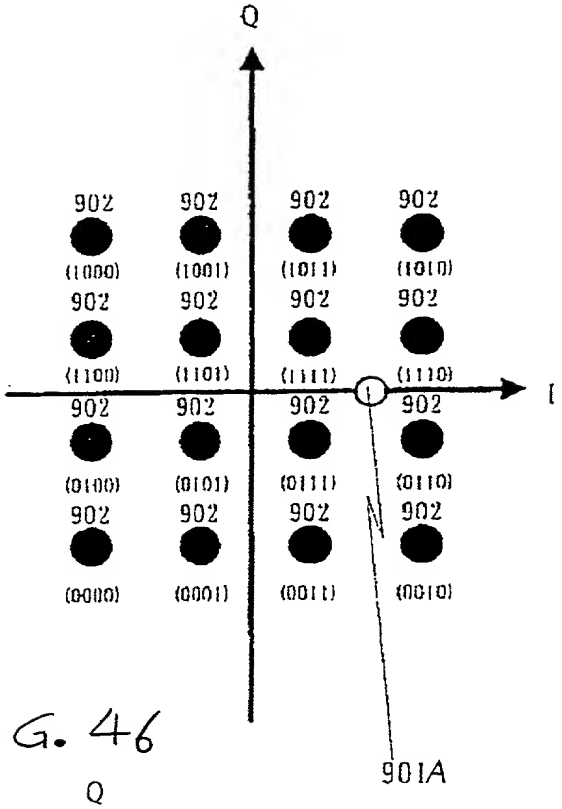
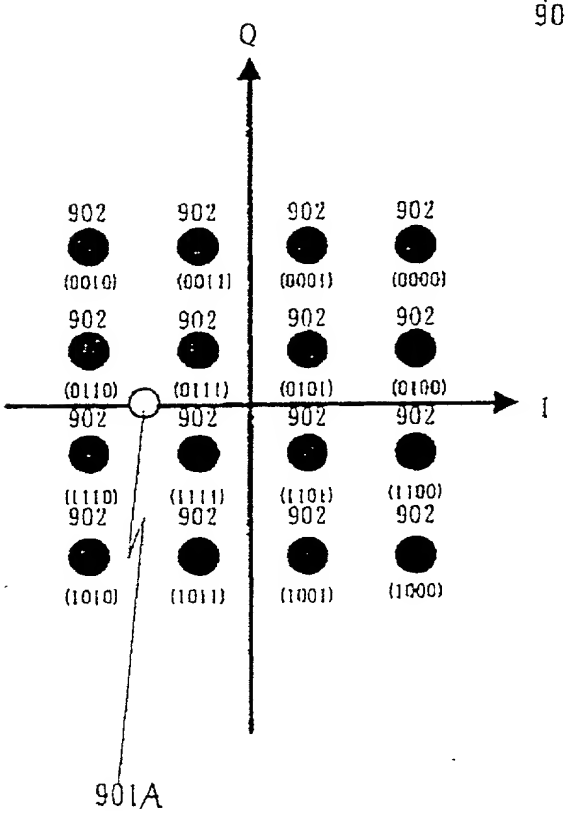


FIG. 46



09540396 - 020196

FIG. 47

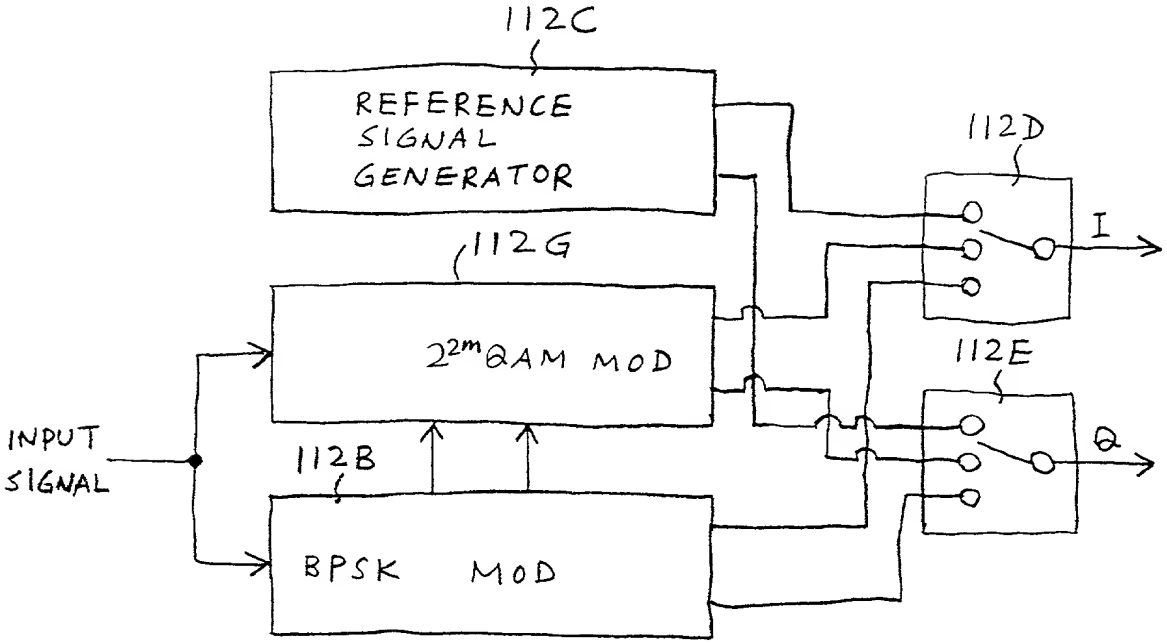

112C
REFERENCE SIGNAL GENERATOR
112D
I
112G
2^{2m}QAM MOD
112E
Q
INPUT SIGNAL
112B
BPSK MOD

FIG. 48

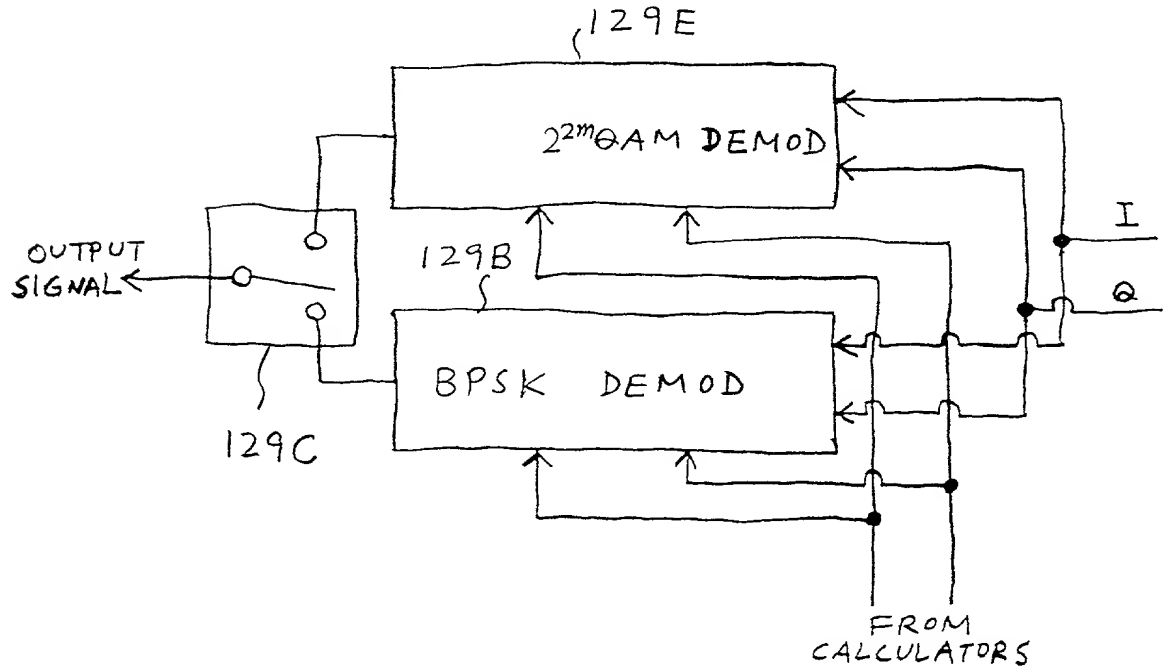

129E
2^{2m}QAM DEMOD
I
Q
OUTPUT SIGNAL
129B
BPSK DEMOD
129C
FROM CALCULATORS

FIG. 49

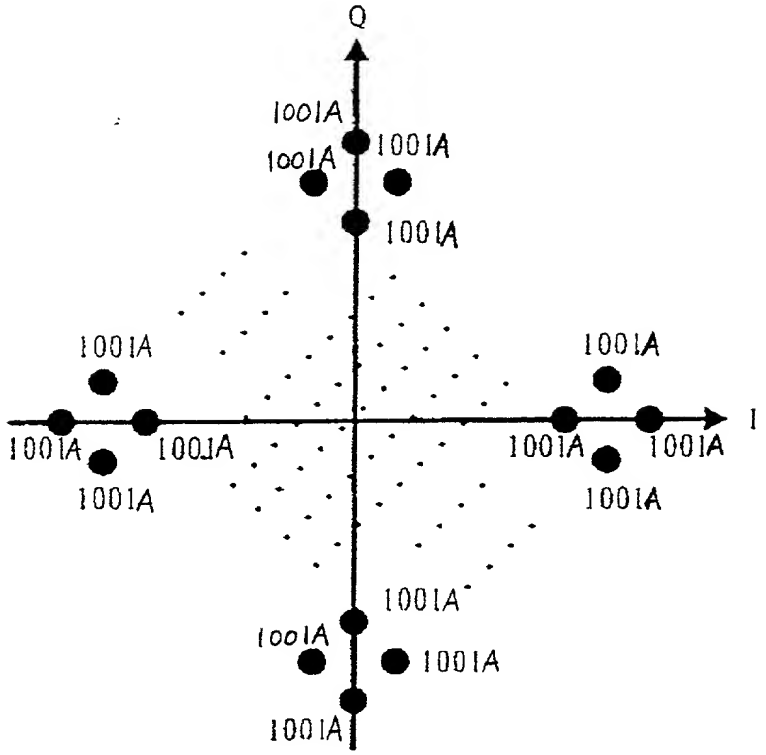

Q
I
1001A
1001A
1001A
1001A
1001A
1001A
1001A
1001A
1001A
1001A
1001A
1001A
1001A
1001A
1001A

FIG. 50

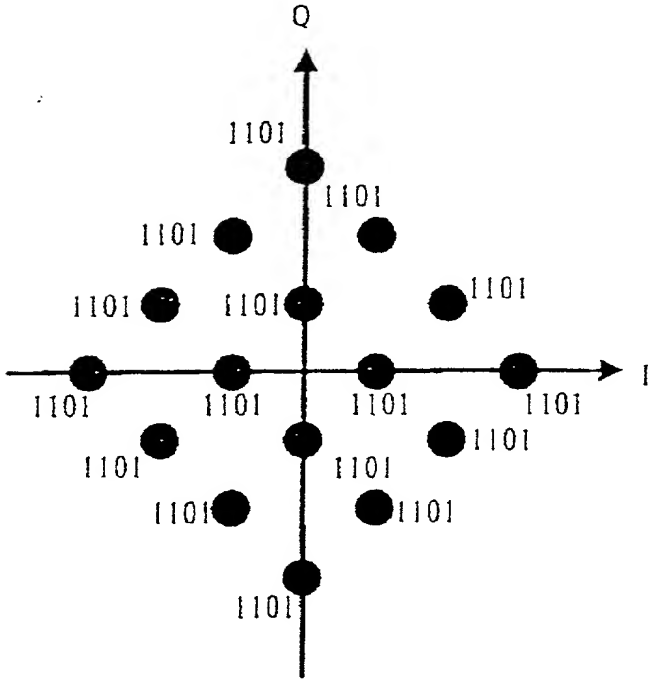

Q
I
1101
1101
1101
1101
1101
1101
1101
1101
1101
1101
1101
1101
1101
1101
1101
1101

FIG. 51

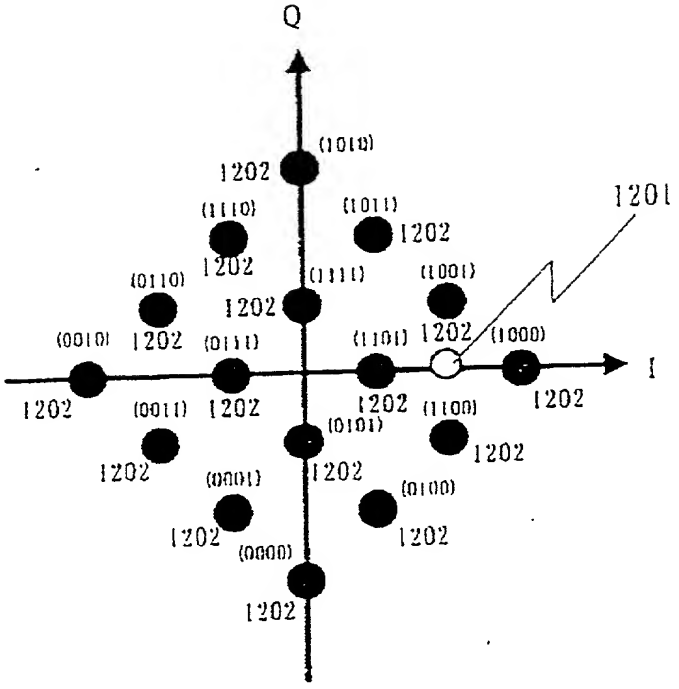

Q
I
1201
1202
(1010)
(1110)
(1011)
(0110)
(1111)
(1001)
(0010)
(0111)
(1101)
(1000)
(0011)
(1100)
(0101)
(0001)
(0100)
(0000)

FIG. 52

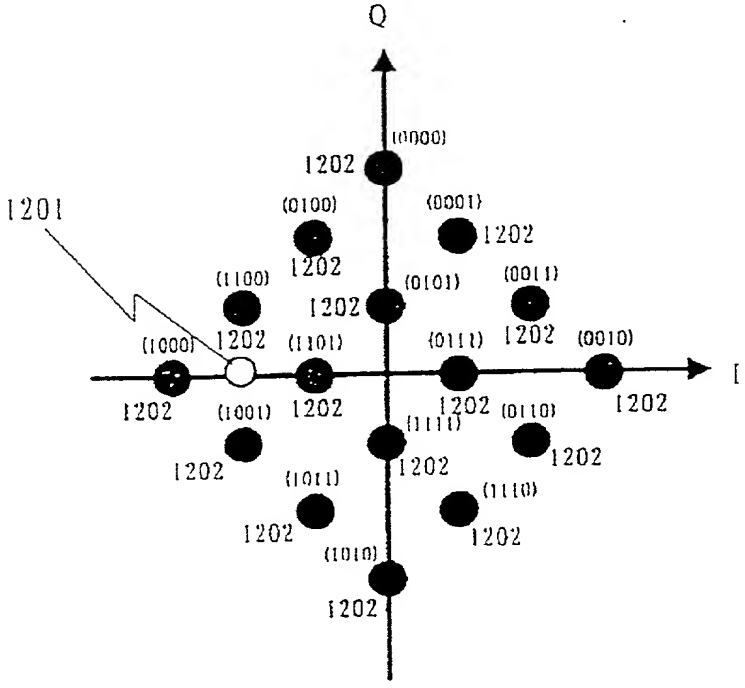

Q
I
1201
1202
(0000)
(0100)
(0001)
(1100)
(0101)
(0011)
(1000)
(1101)
(0111)
(0010)
(1001)
(1111)
(0110)
(1011)
(1110)
(1010)

FIG. 53

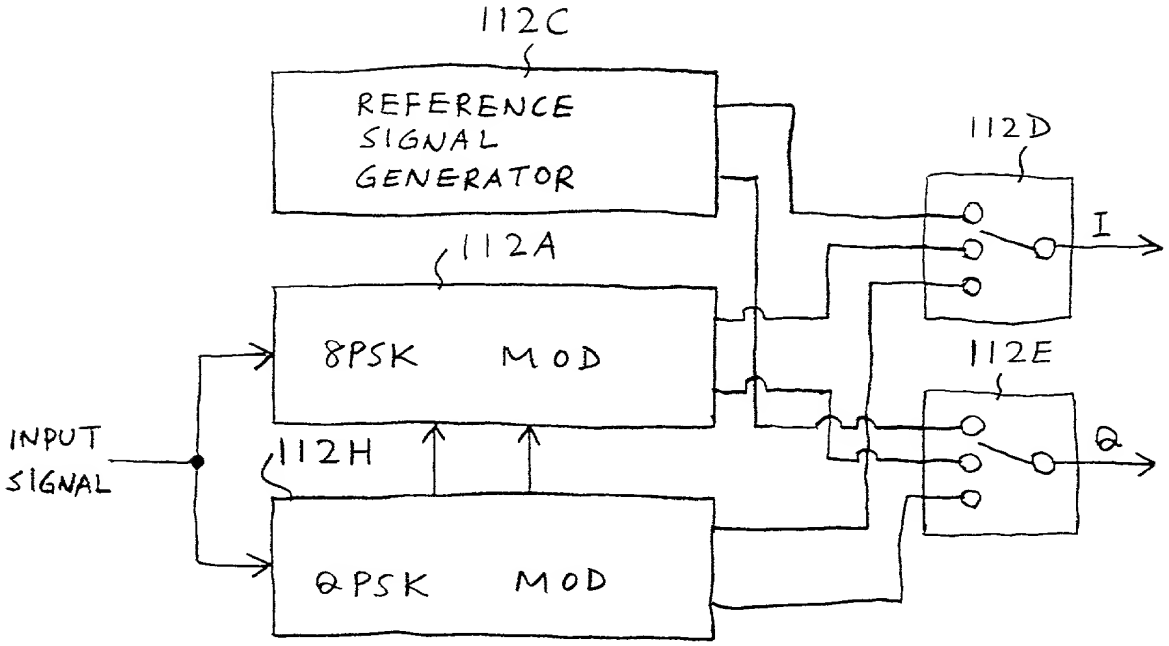

112C
REFERENCE SIGNAL GENERATOR
112D
I
112A
8PSK MOD
112E
Q
INPUT SIGNAL
112H
QPSK MOD

FIG. 54

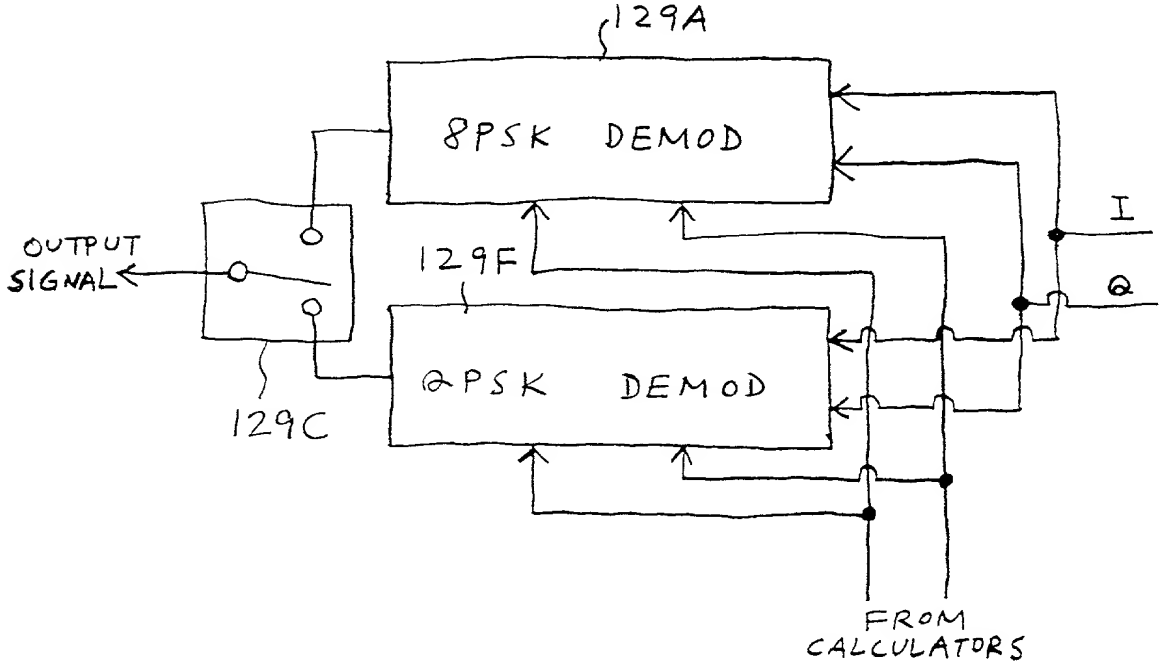

129A
8PSK DEMOD
I
Q
OUTPUT SIGNAL
129F
129C
QPSK DEMOD
FROM CALCULATORS

FIG. 55

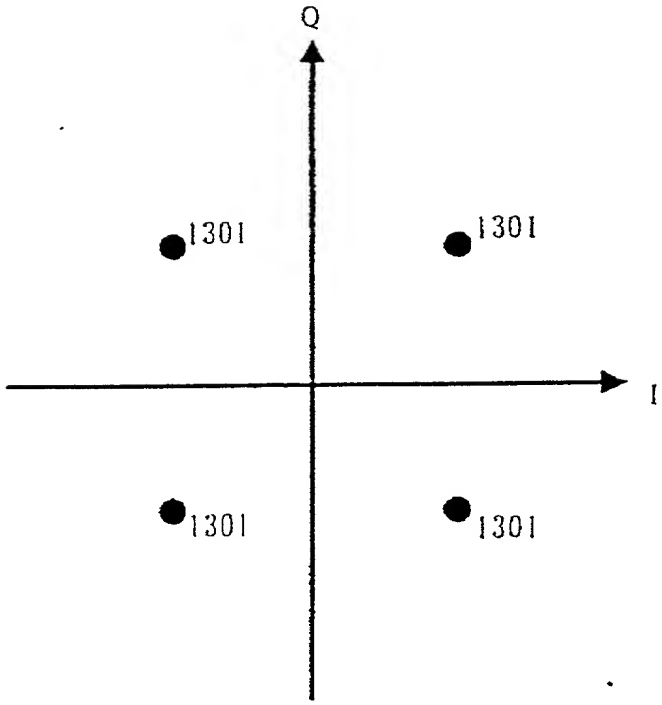


FIG. 56

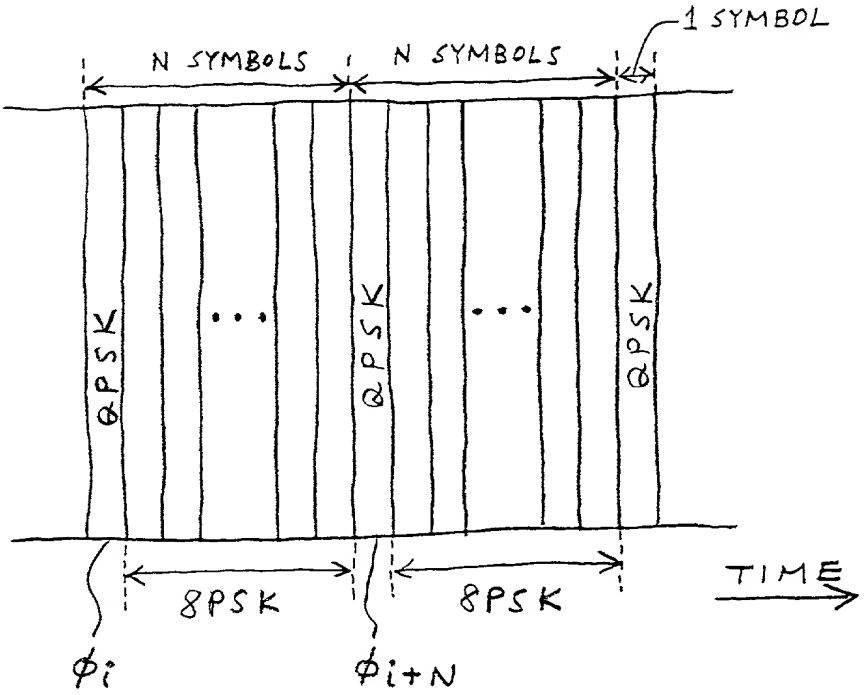

1 SYMBOL
N SYMBOLS
N SYMBOLS
QPSK
QPSK
QPSK
8PSK
8PSK
TIME
φi
φi+N

FIG. 57

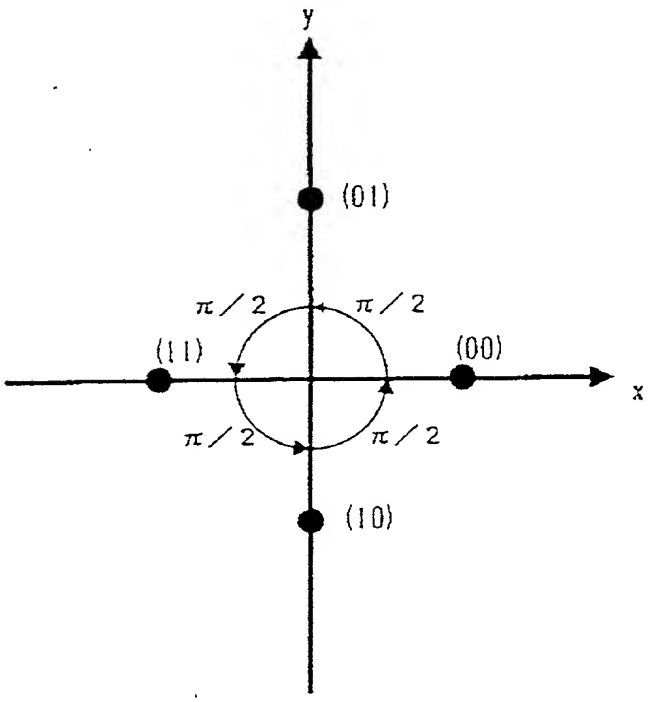

y
(01)
π/2
π/2
(11)
(00)
x
π/2
π/2
(10)

FIG. 58

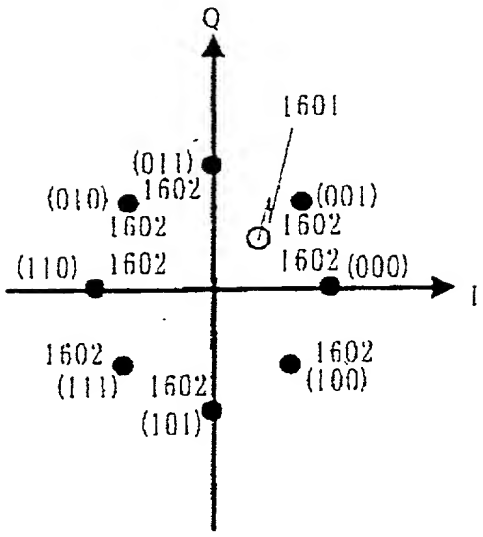


FIG. 59

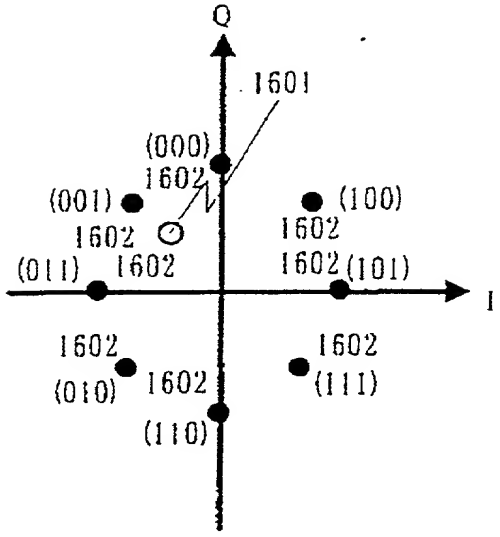


FIG. 60

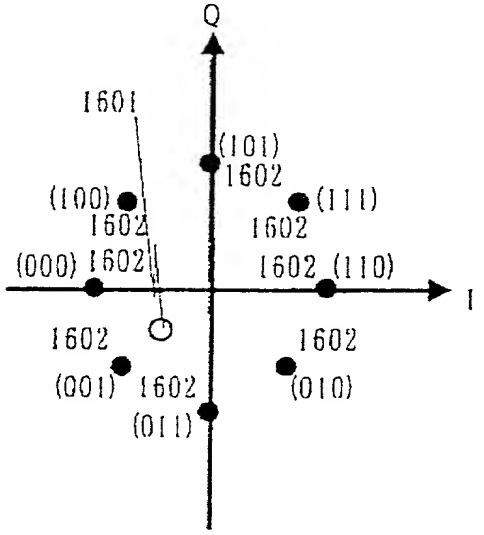


FIG. 61

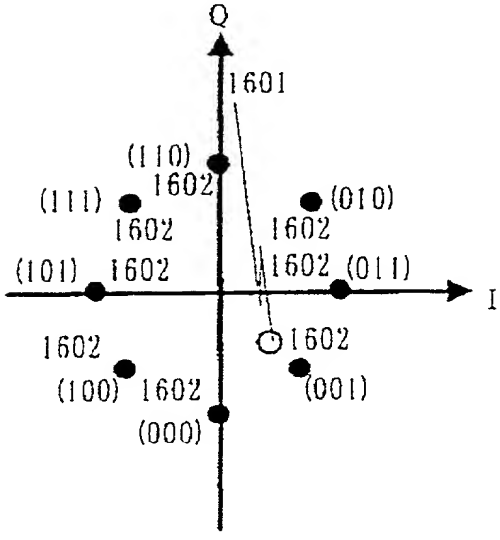


FIG. 62

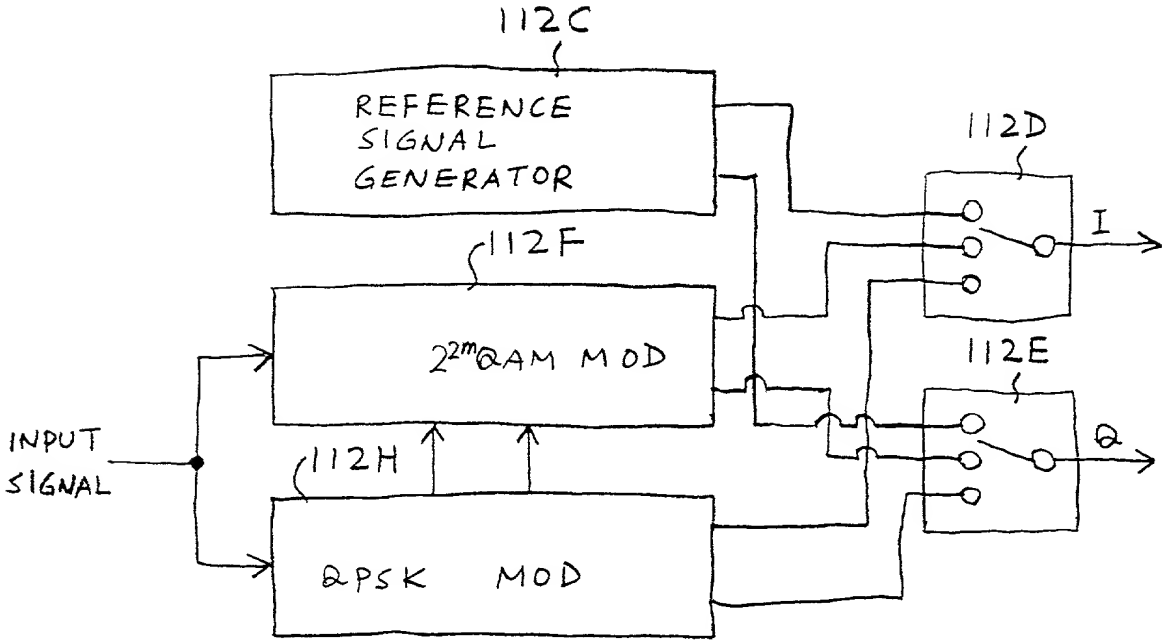

112C
REFERENCE SIGNAL GENERATOR
112D
I
112F
2^{2m}QAM MOD
112E
Q
INPUT SIGNAL
112H
QPSK MOD

FIG. 63

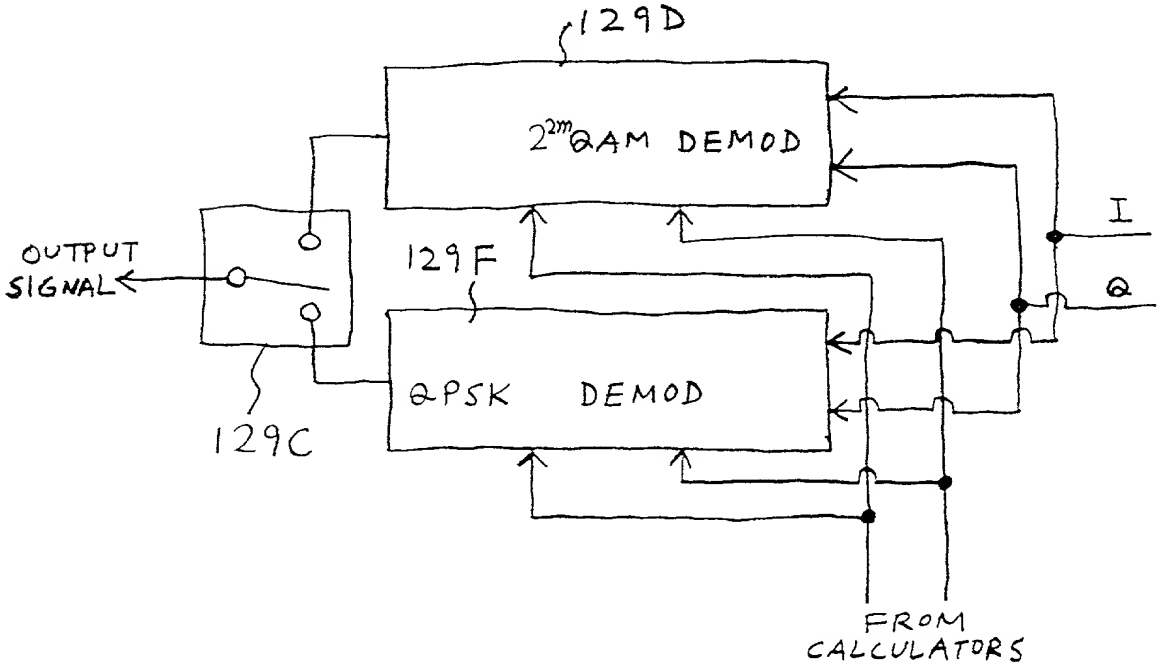

129D
2^{2m}QAM DEMOD
I
Q
OUTPUT SIGNAL
129F
QPSK DEMOD
129C
FROM CALCULATORS

FIG. 64

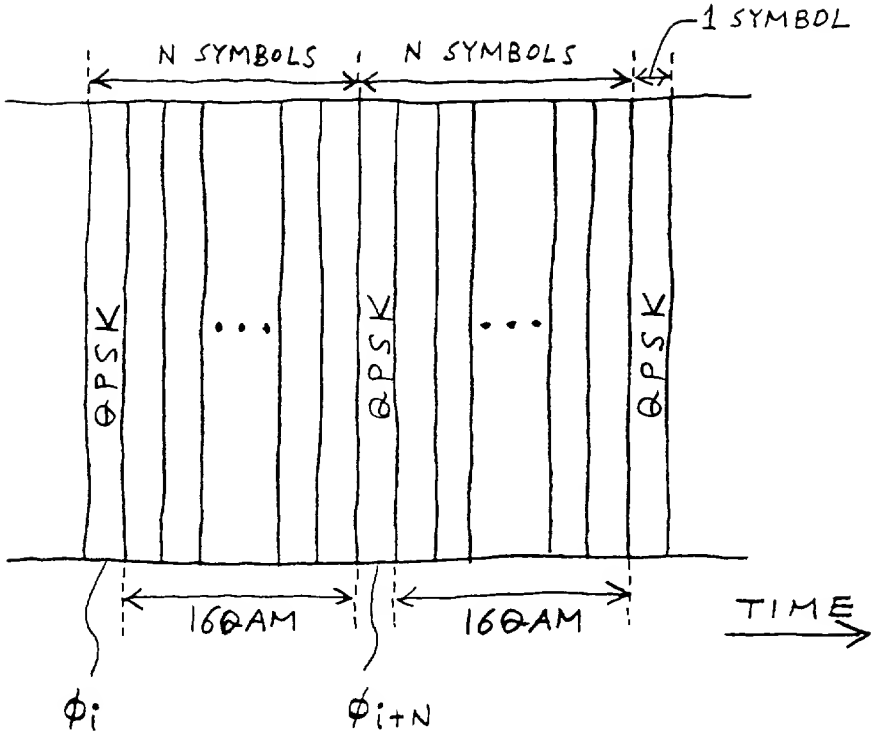

1 SYMBOL
N SYMBOLS
N SYMBOLS
QPSK
QPSK
QPSK
16QAM
16QAM
TIME
ϕ_i
ϕ_{i+N}

FIG. 65

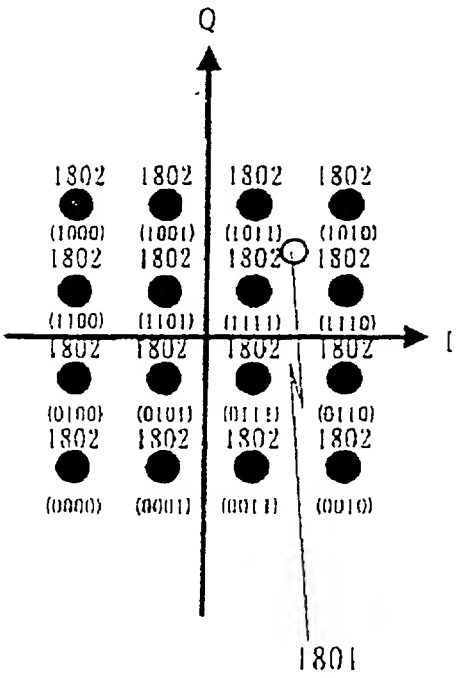


FIG. 66

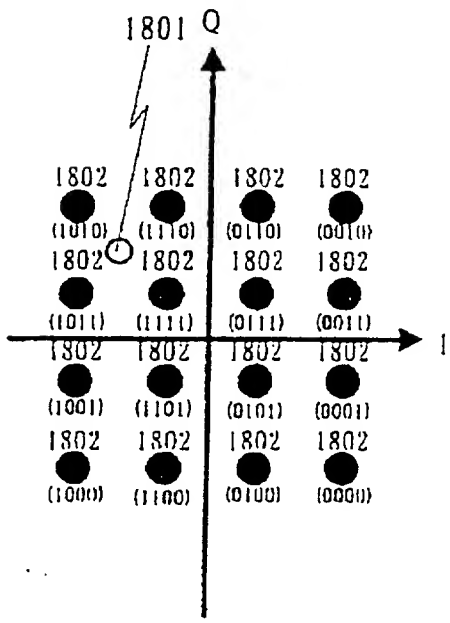


FIG. 67

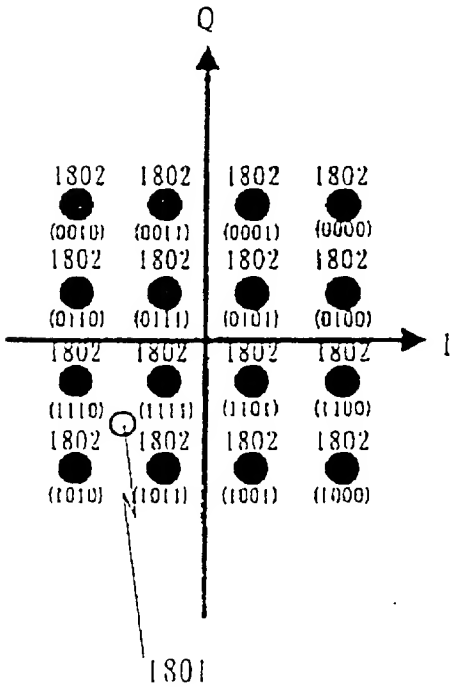
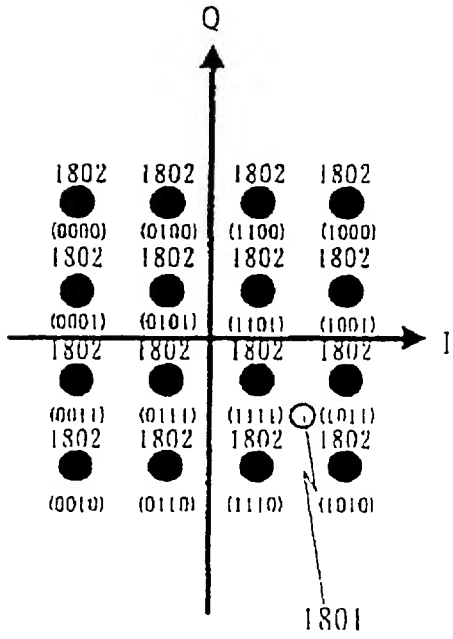


FIG. 68



SCANNED 4

FIG. 69

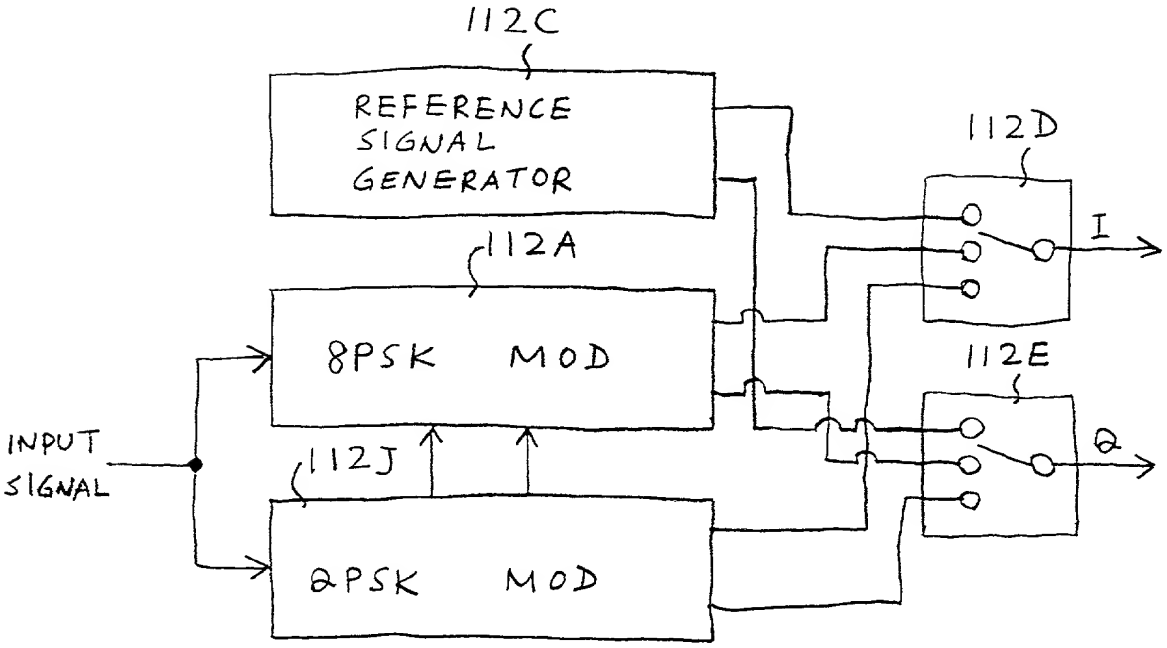
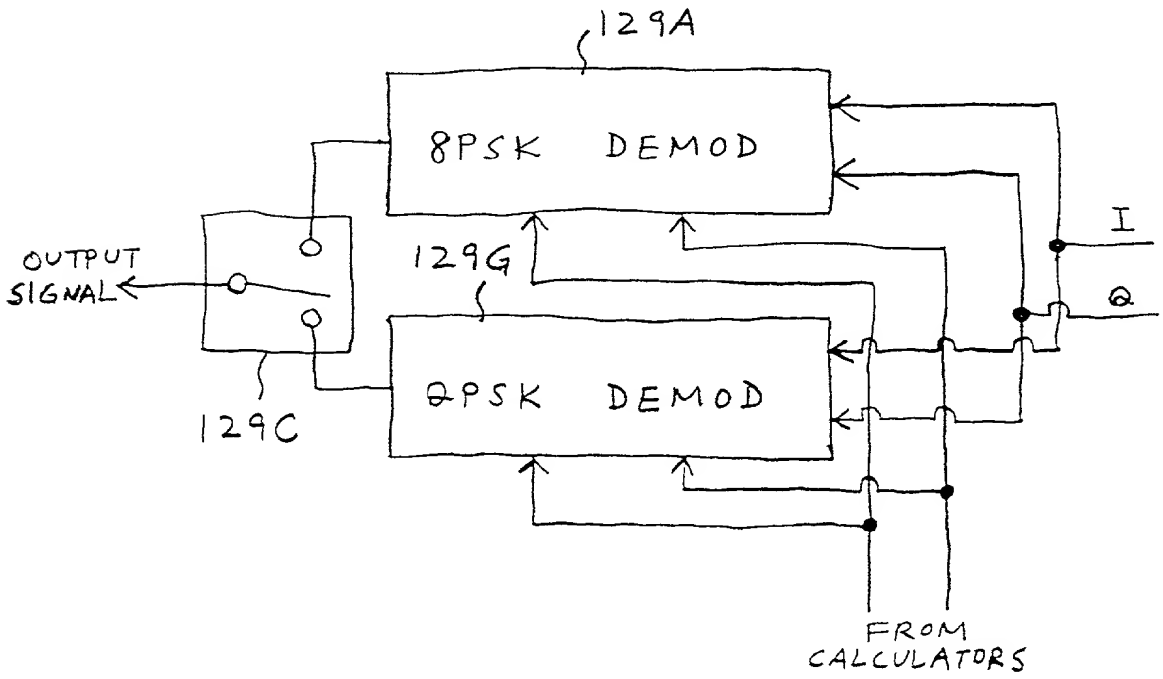
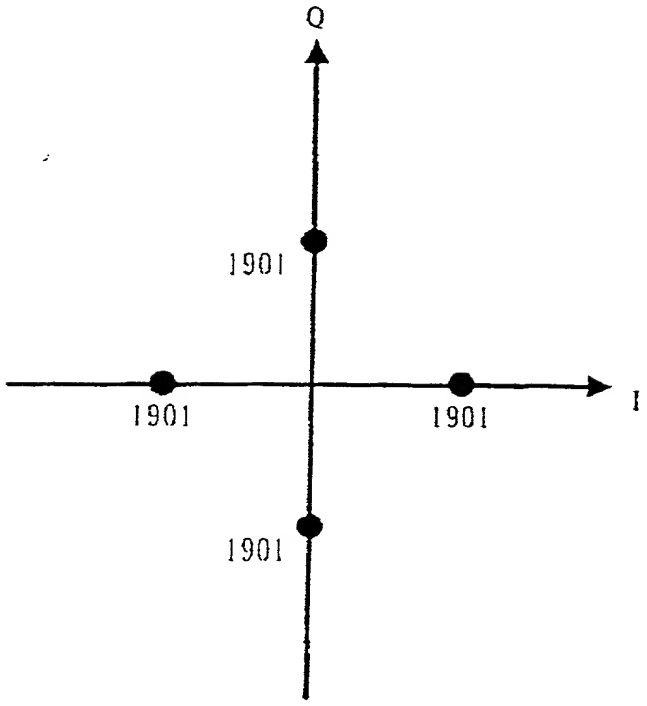


FIG. 70



Sheet 1 of 2 Patent No. 5,768,326

FIG. 71



Substitute Sheet (Rule 26)

FIG. 72

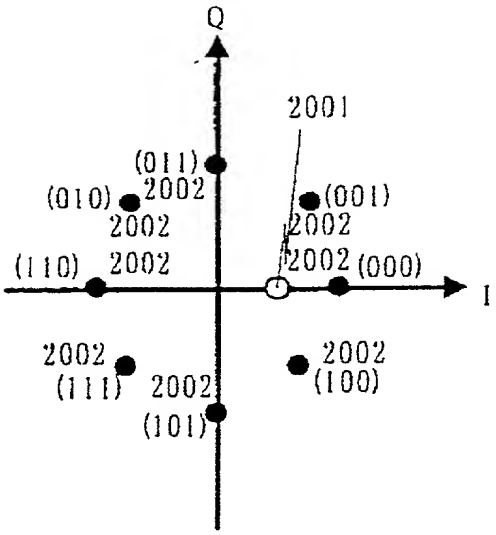


FIG. 73

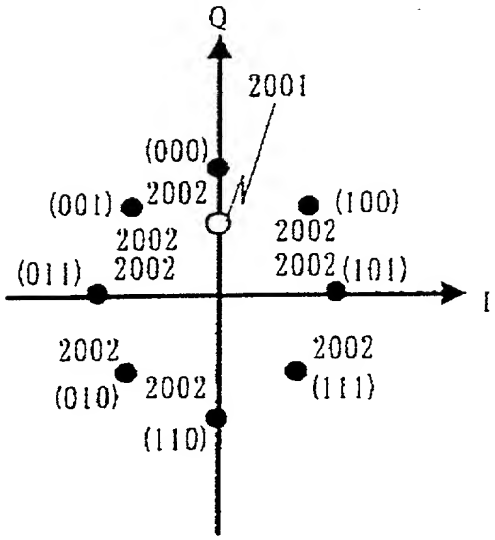


FIG. 74

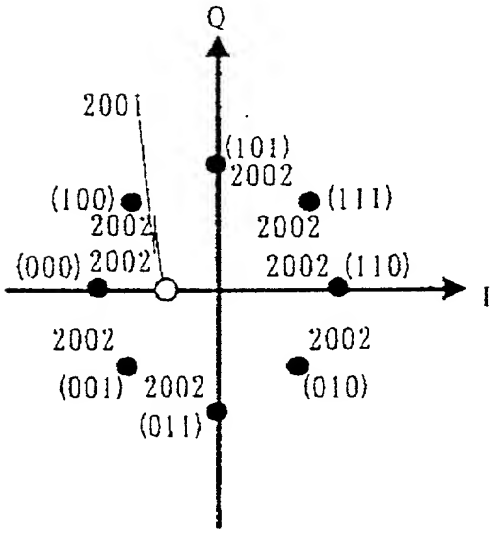


FIG. 75

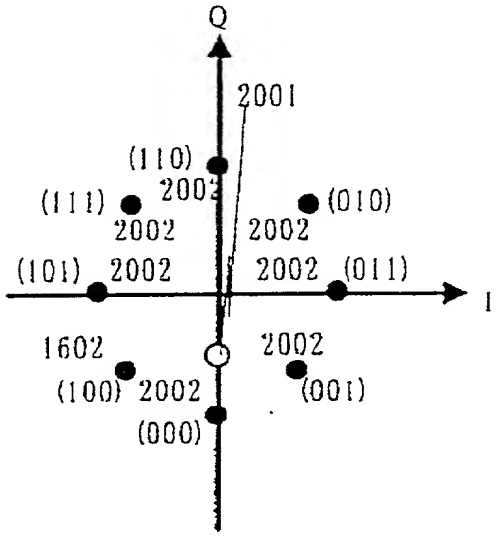


FIG. 76.

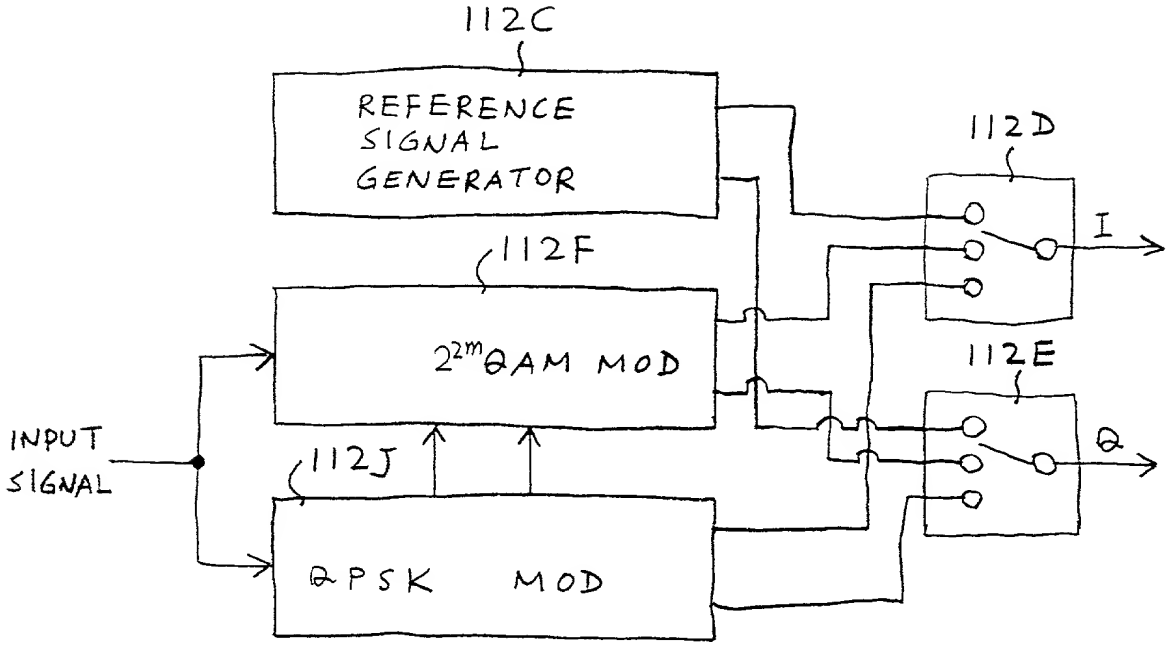

112C
REFERENCE SIGNAL GENERATOR
112D
I
112F
2^{2m}QAM MOD
112E
Q
INPUT SIGNAL
112J
QPSK MOD

FIG. 77

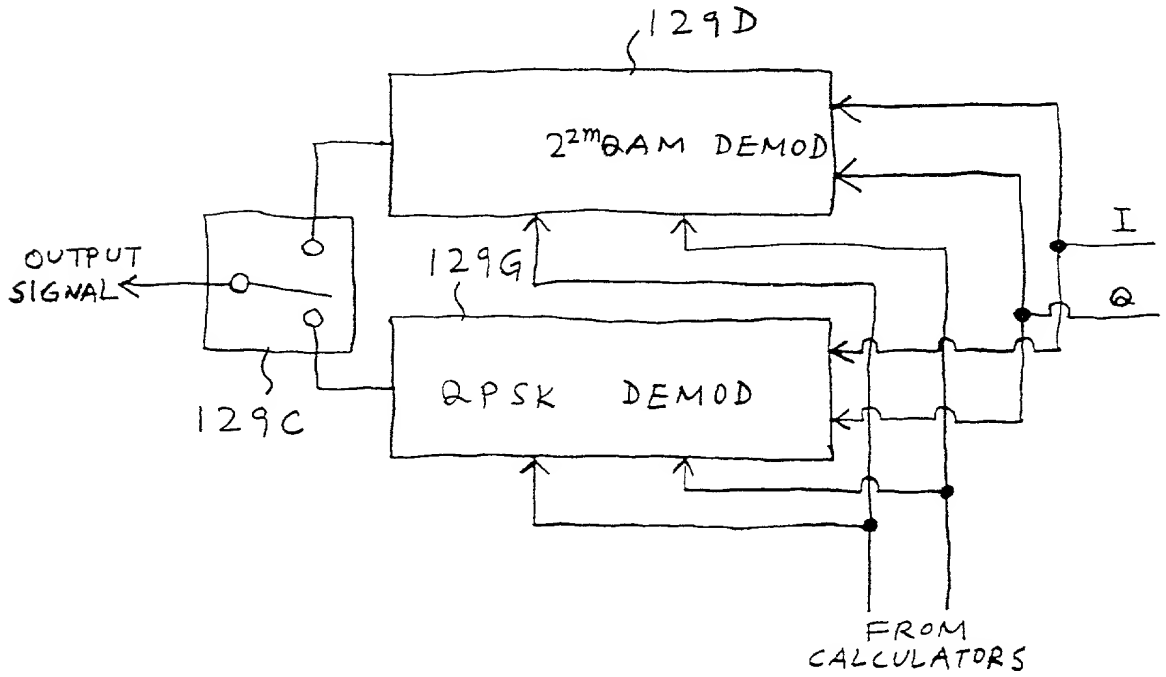

129D
2^{2m}QAM DEMOD
I
Q
OUTPUT SIGNAL
129G
129C
QPSK DEMOD
FROM CALCULATORS

FIG. 78

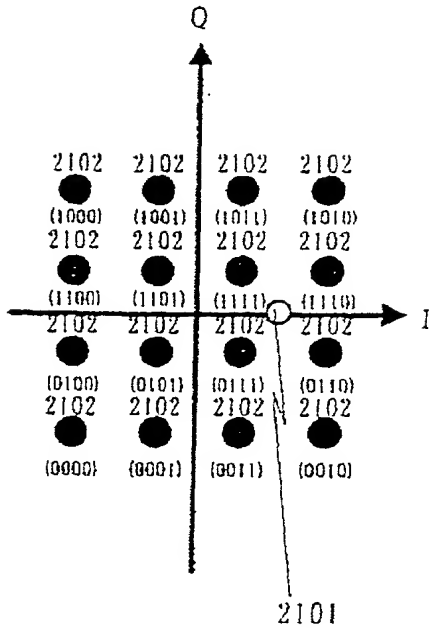


FIG. 79

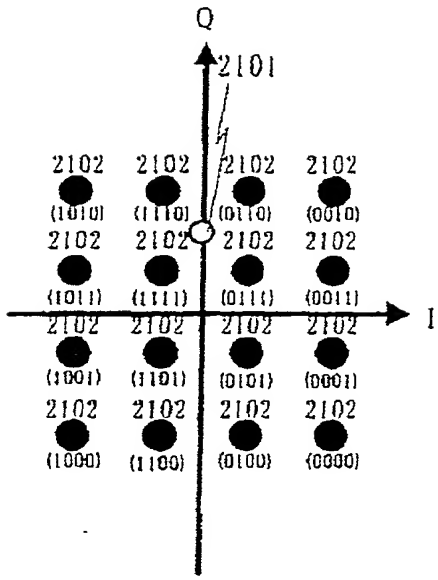


FIG. 80

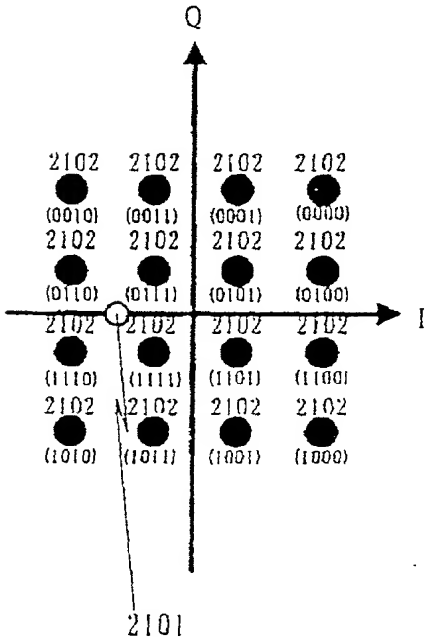
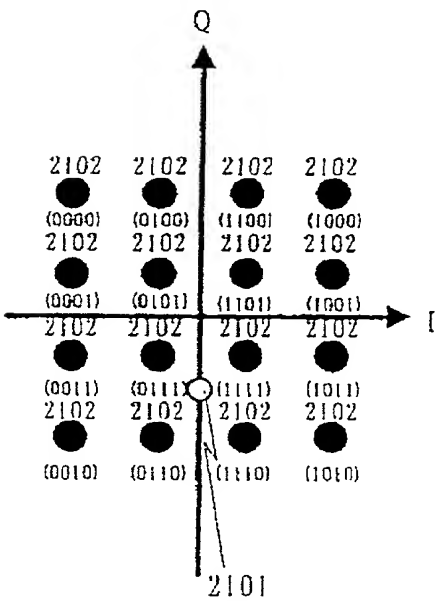


FIG. 81



05250382.0225.US

FIG. 82

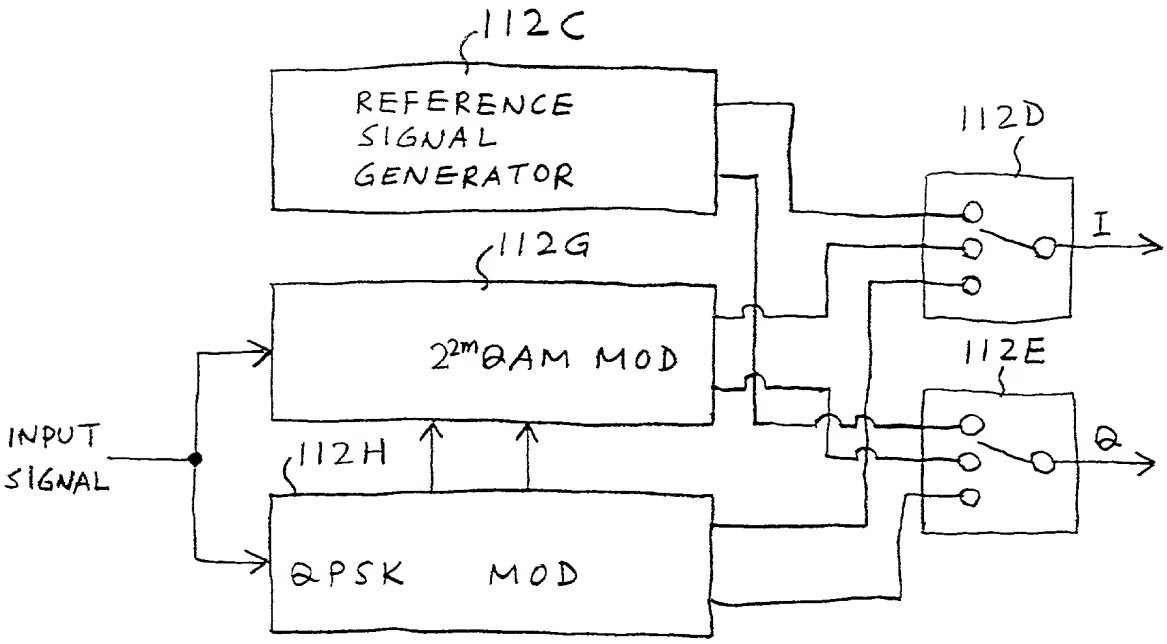

112C
REFERENCE SIGNAL GENERATOR
112D
I
112G
2^mQAM MOD
112E
INPUT SIGNAL
Q
112H
QPSK MOD

FIG. 83

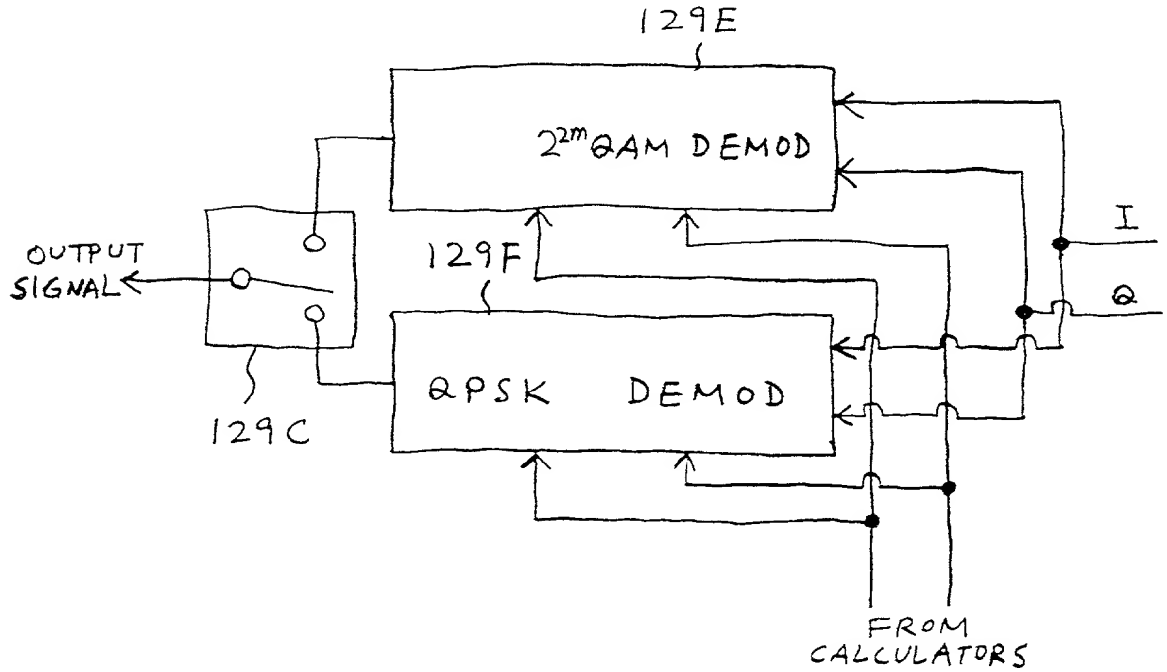

129E
2^mQAM DEMOD
I
OUTPUT SIGNAL
129F
Q
QPSK DEMOD
129C
FROM CALCULATORS

FIG. 84

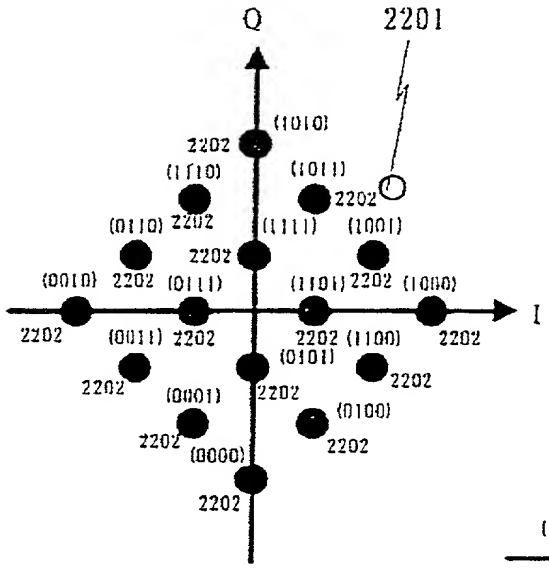


FIG. 85

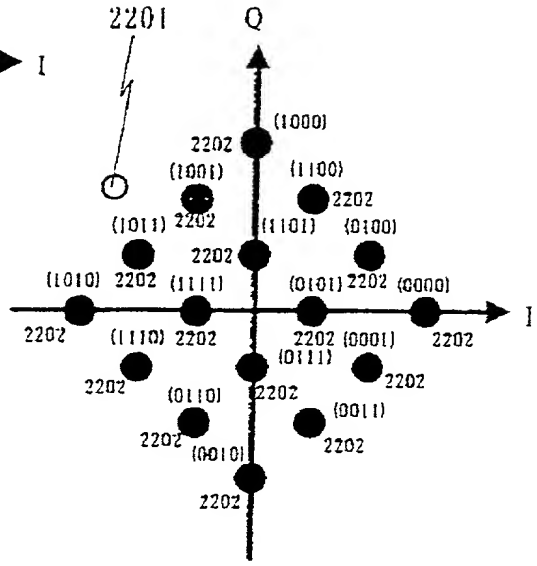


FIG. 86

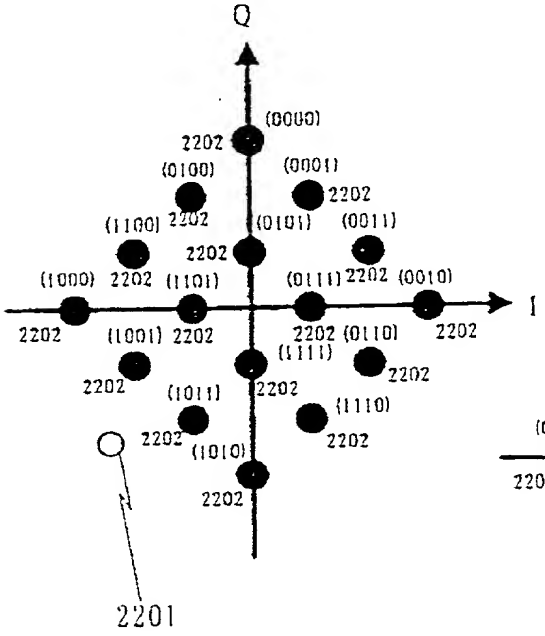
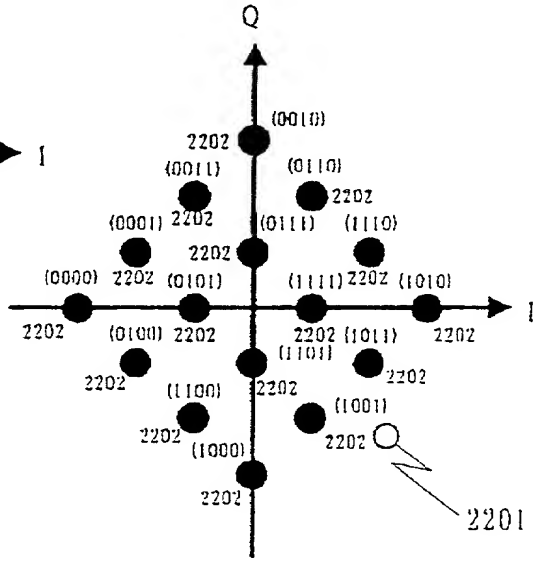


FIG. 87



Substitute Sheet (Rule 26)

FIG. 88

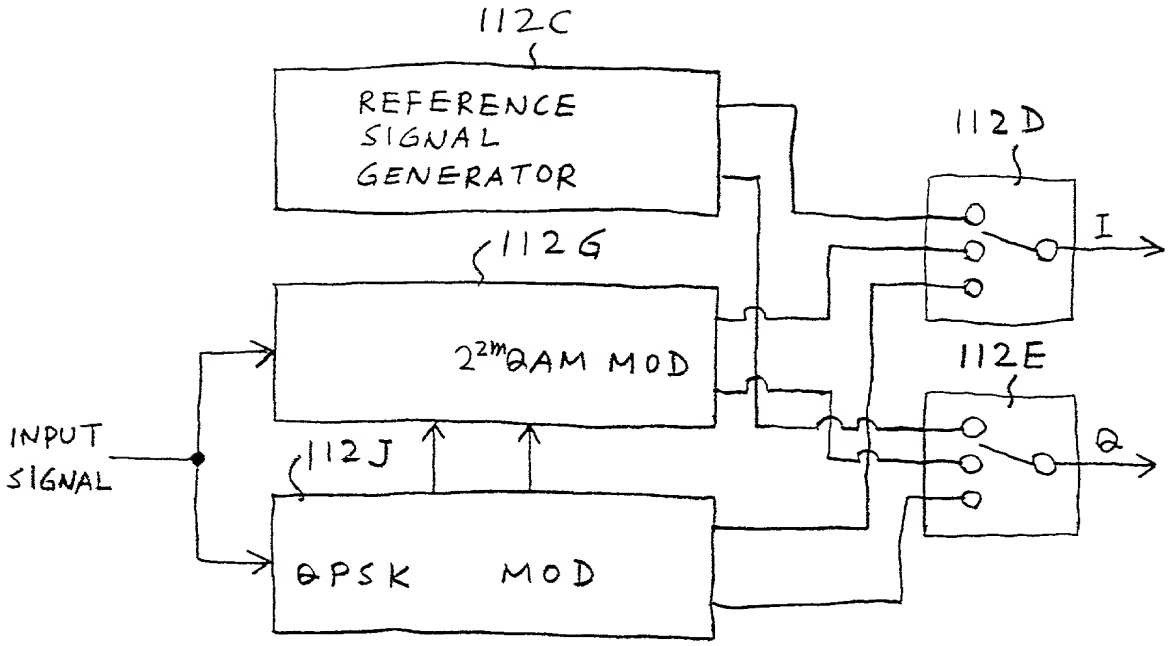
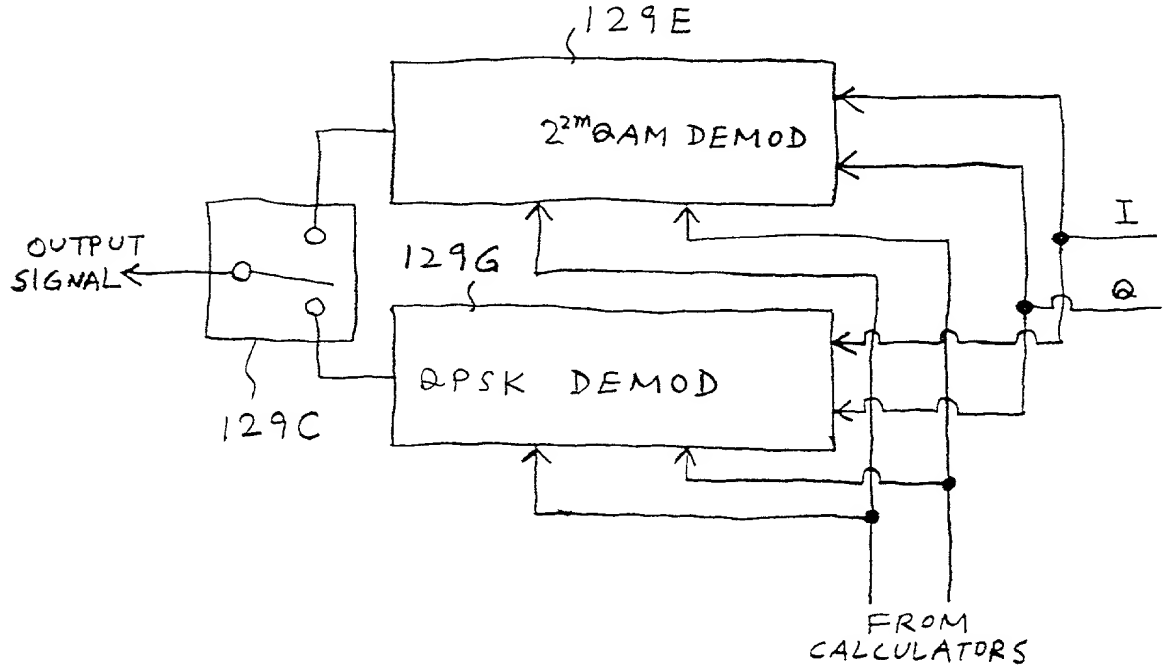


FIG. 89



US 6,359,938 B1

FIG. 90

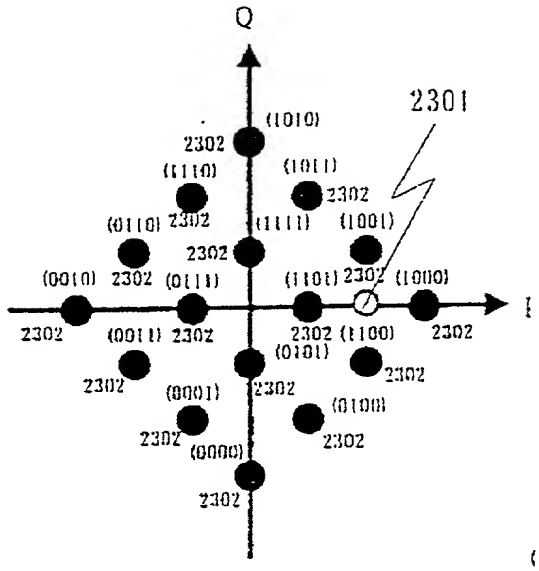


FIG. 91

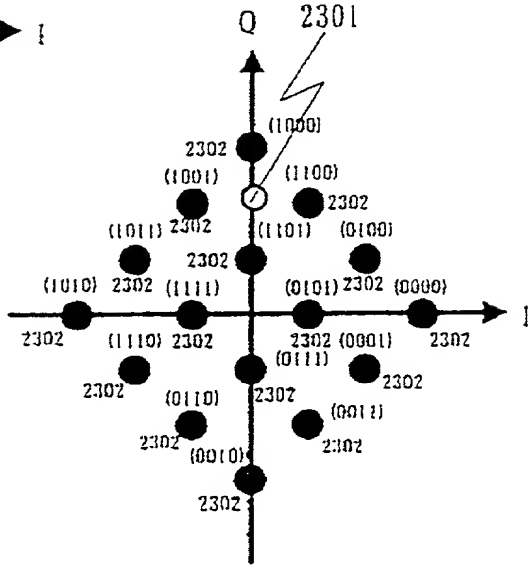


FIG. 92

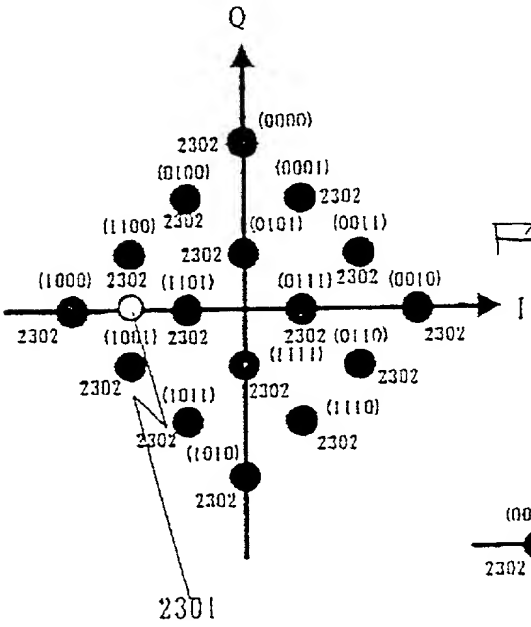


FIG. 93

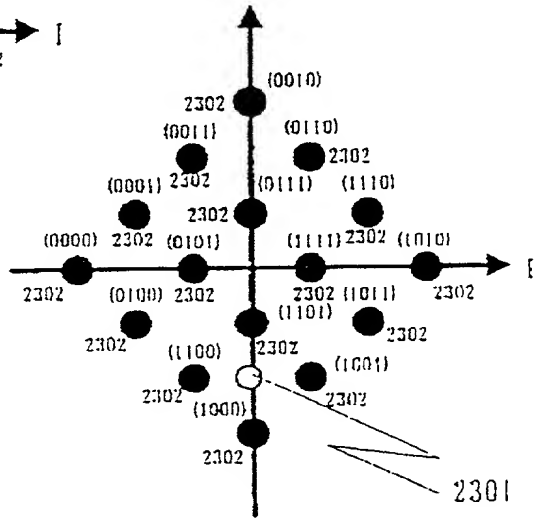
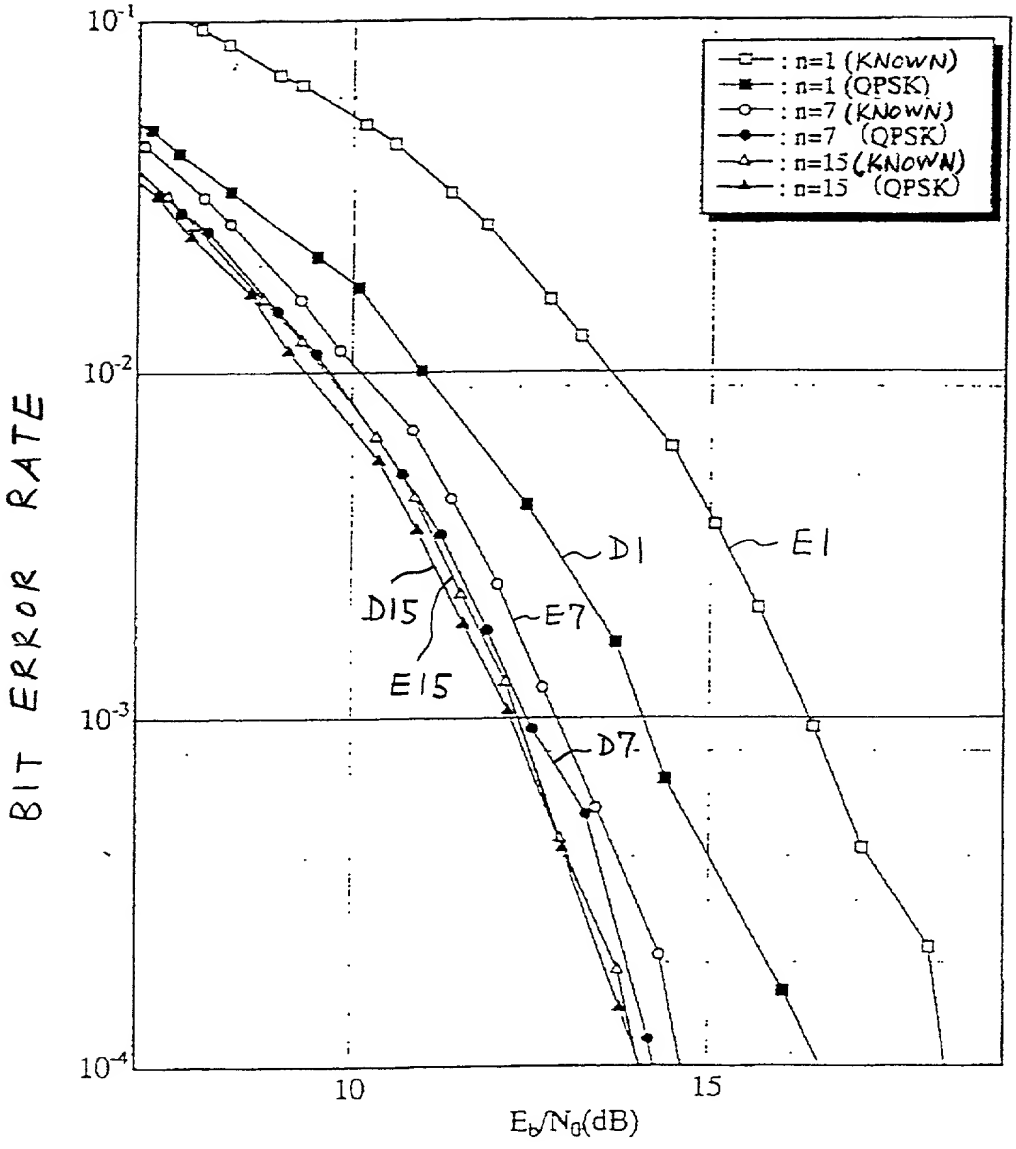


FIG. 94


BIT ERROR RATE
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10
15
E_b/N_0(dB)
: n=1 (KNOWN)
: n=1 (QPSK)
: n=7 (KNOWN)
: n=7 (QPSK)
: n=15 (KNOWN)
: n=15 (QPSK)
D1
E1
D15
E7
E15
D7

P17407-01
US-98110-TH

DECLARATION FOR PATENT APPLICATION

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MODULATION METHOD AND RADIO COMMUNICATION SYSTEM

the specification of which: (check one)

[X] is attached hereto. [ ] was filed on 19__, as United States Patent Application Serial No. or PCT International Application Number _____, and was amended on 19__ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 CFR § 1.56(a).
Prior Foreign Application(s): I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate listed below, or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

(Application No.)	(Country)	(Day/Month/Year Filed)	Priority Claimed
10-18593	Japan	January 30, 1998	[X] [ ] Yes No
10-44983	Japan	February 26, 1998	[X] [ ] Yes No
			[ ] [ ] Yes No

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by 35 U.S.C. § 112, first paragraph, I acknowledge the duty to disclose material information as defined in 37 CFR § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(U.S. Application Serial No.)	(U.S. Filing Date)	(Status--patented, pending, abandoned)

I hereby appoint Elliott I. Pollock, Registration No. 16,906; George Vande Sande, Registration No. 17,276; Burton A. Amernick, Registration No. 24,852; Stanley B. Green, Registration No. 24,351; Richard Wiener, Registration No. 18,741; Townsend M. Belser, Jr., Registration No. 22,956; Morris Liss, Registration No. 24,510; Martin Abramson, Registration No. 25,787; George R. Pettit, Registration No. 27,369; Elzbieta Chlopecka, Registration No. 32,767; Eric J. Franklin, Registration No. 37,134; and Jeffri A. Kaminski, Reg. No. 42,709, my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Send Correspondence and Direct Telephone Calls to:
Morris Liss
(202) 331-7111

Morris Liss
Pollock, Vande Sande & Amernick, R.L.L.P.
P.O. Box 19088
Washington, D.C. 20036-3425 U.S.A.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: Yutaka Murakami
Inventor's Signature Yutaka Murakami Date January 19, 1999
Residence Address Yokohama, Japan
Citizenship Japanese
Post Office Address 2-7-3, Kitaterao, Tsurumi-ku, Yokohama 230-0074 Japan

[X] See next page for additional inventors

DECLARATION FOR PATENT APPLICATION

Full name of second joint inventor (if any): Masayuki Orihashi
Inventor's Signature Masayuki Orihashi Date January 19, 1999
Residence Address Ichikawa-shi, Chiba-ken, Japan
Citizenship Japanese
Post Office Address 1-12-1-302, Futamata,Ichikawa-shi, Chiba-ken 272-0001 Japan

Full name of third joint inventor (if any): Akihiko Matsuoka
Inventor's Signature Akihiko Matsuoka Date January 19, 1999
Residence Address Yokohama, Japan
Citizenship Japanese
Post Office Address 2108-1-201, Kitahassaku-cho,Midori-ku, Yokohama 226-0021 Japan

Full name of fourth joint inventor (if any): Morikazu Sagawa
Inventor's Signature Morikazu Sagawa Date January 19, 1999
Residence Address Tokyo, Japan
Citizenship Japanese
Post Office Address 2-3-15, Nagamine, Inagi-shi, Tokyo 206-0821 Japan

Full name of fifth joint inventor (if any): _____
Inventor's Signature _____ Date _____
Residence Address _____
Citizenship _____
Post Office Address _____

Full name of sixth joint inventor (if any): _____
Inventor's Signature _____ Date _____
Residence Address _____
Citizenship _____
Post Office Address _____

Full name of seventh joint inventor (if any): _____
Inventor's Signature _____ Date _____
Residence Address _____
Citizenship _____
Post Office Address _____

Full name of eighth joint inventor (if any): _____
Inventor's Signature _____ Date _____
Residence Address _____
Citizenship _____
Post Office Address _____

SONY 8193.0